UNIVERSIDAD MIGUEL HERNÁNDEZ DE ELCHE
SPACE POWER AND ELECTRONIC SYSTEMS (*SPES*)

SOLAR ARRAY TO HIGH VOLTAGE BUS: RESONANT POWER CONVERSION TECHNIQUES FOR SPACE APPLICATIONS

PHD THESIS
2025

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This doctoral thesis is supported by a compendium of works published previously in impact scientific journals, indexed according to JCR Science Edition. The main part of this thesis is composed by the following articles, which complete bibliography are listed below:

- *Sequential Switching Shunt Regulation Using DC Transformer for Solar Array Power for Solar Array Power Processing in High Voltage Satellites*
  C. Orts, A. Garrigós, D. Marroquí, A. Franke
  IEEE Transactions on Aerospace and Electronics Systems, Vol. 60, no 1, pp. 421-429. Date of publication: 17 October 2023
  ISSN: 1557-9603
  JCR-SCI Impact Factor: 5,1, Quartile: Q1
  DOI: 10.1109/TAES.2023.3325314

- *Enabling High-Power Conditioning and High-Voltage Bus Integration Using Series-Connected DC Transformers in Spacecrafts*
  C. Orts, A. Garrigós, D. Marroquí, A. Arrizabalaga, A. Franke
  Aerospace, Vol. 11, no 8, 690. Date of publication: 21 August 2024
  ISSN: 2226-4310
  JCR-SCI Impact Factor: 2,1, Quartile: Q2
  DOI: 10.3390/aerospace11080690

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AUTORIZACIÓN DE PRESENTACIÓN DE TESIS DOCTORAL POR UN CONJUNTO DE PUBLICACIONES

Director: Dr. Ausiàs Garrigós
Codirector: Dr. David Marroquí Sempere

Título de la tesis: **Solar array to high voltage bus: resonant power conversion techniques for space applications**

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Universidad Miguel Hernández de Elche

El director y codirector de la tesis reseñada autorizan su publicación en la modalidad de conjunto de publicaciones.

En Elche, a de de 2025

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PROGRAMA DE DOCTORADO EN
TECNOLOGÍAS **I**NDUSTRIALES Y DE
TELECOMUNICACIÓN

Dr. D. German Torregrosa Penalva, Coordinador del Programa de Doctorado en Tecnologías Industriales y de Telecomunicación de la Universidad Miguel Hernández de Elche.

Certifica

Que el trabajo realizado por D. Carlos Orts Torres titulado **Solar array to high voltage bus: resonant power conversion techniques for space applications** ha sido dirigido por el Dr. Ausiàs Garrigós Sirvent y codirigido por el Dr. David Marroquí Sempere y se encuentra en condiciones de ser leído y defendido como Tesis doctoral ante el correspondiente tribunal en la Universidad Miguel Hernández de Elche.

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Agradecimientos

La redacción de la presente tesis doctoral marca un punto final a tres años de dedicación y trabajo constante, que, de una forma u otra, ha requerido el apoyo de un gran número de personas, porque nadie camina solo.

En primer lugar, agradezco a mis directores de tesis Ausiàs Garrigós Sirvent y David Marroquí Sempere en haberme dado la oportunidad y confianza de haber trabajado en un proyecto tan apasionante junto a ellos. Sus aportaciones y visiones me han permitido aprender día a día.

Después, doy las gracias al resto de miembros del grupo de investigación SPES: José Manuel Blanes, José António Carrasco y Javier Rubiato; así como a los compañeros del Área de Tecnología Electrónica por darme su apoyo, sabiduría y, sobre todo, su simpatía.

A mis muy estimados compañeros de laboratorio: Cristian, Pablo, David, Diego y Andrea, les agradezco por tantas horas que hemos pasado juntos ya sea trabajando, tomando café o teniendo conversaciones de lo más agradables. Espero seguir encontrándome a compañeros igual que vosotros.

I would like to especially thank to Andreas Franke for being our technical officer and providing such valuable expertise to help us develop this project. Also, I like to thank all the people of TEC-EPM for their friendly reception during my research stay, and especially the ones I had the opportunity to work with: Pablo, Oliver, Antxon, Valentin and Theyllor.

A mis padres y a mis hermanos, les doy las gracias de todo corazón por todo su apoyo incondicional durante todos estos años, que han sabido ayudarme en todo momento y han ido empujándome hacía la dirección correcta. Porque sin ellos, esta tesis no hubiera sido posible.

También agradezco a todos mis amigos por su apoyo, sin importar si se encuentran en Elche o desperdigados por el resto del mundo, siempre nos volvemos a juntar.

A todas las personas que no pude incluir y que han contribuido de alguna forma a esta tesis, les doy las gracias.

De ahí para arriba

Resumen

La evolución del cambio climático durante las últimas décadas ha llevado a la exploración de nuevos métodos de generación eléctrica sin emisiones de CO_2. Una posible solución es desplegar plataformas de energía solar espacial, que supondría utilizar grandes estructuras de paneles solares en órbita capaces de generar electricidad en el orden de GW y transmitirla a estaciones terrenas conectadas a la red eléctrica. Durante los últimos años, diferentes naciones alrededor del mundo, incluyendo los Estados Unidos de América, China y Japón, han iniciado programas para investigar y desarrollar plataformas comerciales de Energía Solar Basada en el Espacio (SBSP). En Europa, la Agencia Espacial Europea (ESA) ha promovido la iniciativa SOLARIS, que busca establecer la viabilidad, el conocimiento fundamental y las tecnologías necesarias para el desarrollo de un demostrador orbital.

Para poder procesar y distribuir la potencia de forma efectiva y viable desde las secciones de paneles solares hacia el resto de la plataforma, es necesario disponer de un bus de distribución de alta tensión capaz de alcanzar hasta 20 kV. Las topologías convencionales basadas en la transferencia directa de energía mantienen las secciones de paneles solares a la misma tensión que el bus de distribución. Sin embargo, este tipo de métodos no resulta apropiado para la gestión directa de la potencia en el orden de GW. En la actualidad, la tensión máxima de las secciones de los paneles solares alcanza 120 V, debido a la aparición de efectos de alta tensión a mayores voltajes en entornos espaciales, que degradan de forma significativa las celdas solares. Por lo tanto, es necesario disponer de un sistema de potencia capaz de convertir la baja tensión de los paneles fotovoltaicos en buses de distribución de alta tensión.

Dado el contexto y la necesidad de soluciones respecto a la gestión y distribución de potencia en plataformas de alta tensión, el objetivo de esta tesis doctoral es proponer y desarrollar una arquitectura novel para la conversión y regulación de la tensión para las secciones de paneles solares, basado en dos reconocidas técnicas en el sector espacial: el Regulador Shunt de Conmutación Secuencial (S3R) y el convertidor resonante en tensión y corriente (ZVZC) de ganancia fija (DCX).

El primer capítulo corresponde a los aspectos académicos respecto al Programa de Doctorado en Tecnologías Industriales y de Telecomunicación (TECNIT) de la Universidad Miguel Hernández de Elche.

En el segundo capítulo se presenta el contexto del sistema eléctrico de potencia de los satélites, los efectos de alta tensión en entornos espaciales, y el estado del arte de las plataformas SBSP y sus requisitos eléctricos.

El tercer y cuarto capítulo se corresponden a los dos artículos de revistas que conforman el compendio de artículos de la tesis doctoral. Además de los artículos, los resultados han sido desarrollados y analizados en profundidad, siendo los principales temas tratados mostrados a continuación:

- Se valida una nueva técnica de regulación de paneles solares para satélites de alta tensión, denominado Regulador Shunt de Conmutación Secuencial DCX (S3DCX). Se analiza el principio de funcionamiento y se modela el sistema. A continuación, se describe una metodología de diseño y se construye un prototipo de 2 kW destinado a secciones de paneles solares de 100 V y tensión de salida de 300 V. El sistema se desarrolla en base a los requerimientos establecidos por *European Cooperation for Space Standardization* (ECSS) de la ESA para buses de distribución regulados.

- Se realiza un análisis exhaustivo de los semiconductores de potencia disponibles y compatibles para aplicaciones de alta tensión en entornos de radiación espacial. Se desarrolla un análisis experimental para incrementar las capacidades de potencia del S3DCX basado en semiconductores de banda ancha prohibida. Se valida y estudia la modularidad de las celdas de potencia para alcanzar tensiones de bus regulado a 600 V y 900 V. También se estudia el aislamiento eléctrico de los transformadores y de la celda de potencia en condiciones de vacío.

El último capítulo de la tesis se presentan sus conclusiones, se resumen las principales contribuciones y se proponen futuras líneas de investigación.

Por último, la tesis se cierra con cinco anexos que proporcionan detalles respecto al software desarrollado, los esquemáticos de los prototipos y una descripción de los bancos de trabajo.

Abstract

The evolution of climate change over the last decades has led to the exploration of new methods of generating electricity without CO_2 emissions. One potential solution is the deployment of space-based solar power (SBSP) platforms, which involves the use of large solar array structures in orbit capable of generate electricity in the GW range and transmitting it to a ground station connected to the electrical grid. In recent years, several nations worldwide, including the United States of America, China, and Japan, have initiated programmes to research and develop commercial SBSP systems. In Europe, the European Space Agency (ESA) has promoted the SOLARIS initiative, which aims to establish the feasibility, fundamental knowledge, and necessary technology for the development of an orbital demonstrator.

To effectively and reliably distribute power from the solar array sections to the rest of the platform, high voltage distribution buses of up to 20 kV are required. In conventional direct energy transfer topologies, the solar array sections operate at the same voltage as the distribution bus. However, such methods are not well suited to managing power in the GW range. At present, the maximum solar arrays voltage is 120 V, due to the occurrence of several effects in the space environment at high voltage, which significantly degrade the solar cells. It is therefore necessary to have a power system capable of converting the low voltage from the solar array section to the high voltage distribution bus.

Considering the context and the need for power management and distribution solutions for high voltage platforms, the aim of this doctoral thesis is to propose and develop a novel architecture for the voltage conversion and regulation of the solar array sections, based on well established techniques in the space sector: the Sequential Switching Shunt Regulator (S3R) and the Zero Voltage Zero Current Switching (ZVZC) Direct Current Transformer (DCX) converter.

The first chapter deals with the academic aspects of the Doctoral Program in Industrial and Telecommunications Technologies (TECNIT) of the Miguel Hernández University of Elche.

The second chapter presents the context of electrical power systems in satellites, the effects of high voltage in space environments, and an overview of the state of the art in SBSP platforms and their electrical requirements.

The third and fourth chapters correspond to the two journal papers that form the core of this doctoral thesis. In addition to the papers presented, the results are extended and analysed in depth, with the main topics listed below:

- A novel technique for solar array regulation in high voltage satellites, called the Sequential Switching Shunt DCX Regulator (S3DCX), has been validated. The operating principle, modelling, and design methodology have been analysed. A 2 kW prototype for 100 V solar array sections and 300 V output has been developed in accordance with the requirements established from the European Cooperation for Space Standardization (ECSS) of ESA for regulated distribution buses.

- A thorough analysis of the available power semiconductors compatible with high voltage applications in space radiation environments has been conducted. An experimental study was carried out to improve the power capabilities of the S3DCX based on wide bandgap semiconductors. The modularity of the power cells has been studied and validated up to 600 V and 900 V regulated distribution buses. The electrical isolation of the transformer and power cell under vacuum conditions was also studied.

The final chapter of the thesis presents the conclusions, summarising the main contributions of this work and proposing future lines of research.

Lastly, the thesis closes with five annexes containing details of the developed software, the schematics of the prototypes, and a description of the experimental setups.

List of abbreviations

AC	Alternate Current
BCR	Battery Charge Regulator
BDR	Battery Discharge Regulator
BEA	Battery Error Amplifier
CASC	China Aerospace Science and Technology Corporation
CNSA	China National Space Administration
COTS	Commercial Off-The Shelf
DAB	Dual Active Bridge
DC	Direct Current
DCX	Direct Current Transformer
DET	Direct Energy Transfer
ECSS	European Cooperation for Space Standardization
EMI	ElectroMagnetic Interferences
EPC	Electronic Power Conditioner
EPS	Electric Power System
ESA	European Space Agency
ESR	Equivalent Series Resistance
ESTEC	European Space Research and Technology Centre
FET	Field-Effect Transistor
FoM	Figure of Merit
FPGA	Field-Programmable Gate Array
GEO	Geostationary Earth Orbit
HP	High Power
HV	High Voltage
ISAS	Institute of Space and Astronautical Science
ISS	International Space Station
JAXA	Japan Aerospace eXploration Agency
LET	Linear Energy Transfer
LEO	Low Earth Orbit
LEOP	Launch and Early Operation Phase
LV	Low Voltage
MAPLE	Microwave Array Power transfer Low-earth orbit Experiment
MEA	Main Error Amplifier
MKP	Metalized polypropylene
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracker

NASA National Aeronautics and Space Administration
N.C Not Connected
NHFFOM New High Frequency Figure Of Merit

PCB Printed Circuit Board
PCDU Power Conditioning and Distributing Unit
PDU Power Distribution Unit
PCU Power Conditioning Unit
PhD Philosophie Doctor
PI Proportional Integral
PLL Phase-Locked Loop
PPU Power Processing Unit
PSFB Phase-Shift Full Bridge
PWM Pulse Width Modulation

RMS Root Mean Square

S3DCX Sequential Switching Shunt DCX Regulator
S3R Sequential Switching Shunt Regulator
S4R Sequential Switching Shunt Series Regulator
SADM Solar Array Drive Mechanism
SAS Solar Array Section
SBSP Space-Based Solar Power
SEB Single Event Breakdown
SPES Space Power & Electronic Systems
SPS Solar Power Satellite
SSO Sun Synchronous Orbit
SSPA Solid-State Power Amplifier
SSPIDR Space Solar Power Incremental Demonstrations and Research project

TECNIT Doctorate in Industrial and Telecommunications Technologies
TID Total Ionizing Dose
TRL Technology Readiness Level
TWTA Travelling Wave Tube Amplifier

UMH Miguel Hernández University of Elche
U.S United States of America

WBG Wide-BandGap semiconductor

ZCS Zero Current Switching
ZVS Zero Voltage Switching
ZVZC Zero Voltage Zero Current
ZVZCS Zero Voltage Zero Current Switching

Funding

The present PhD thesis was made possible through the funding of the research project, which included a budget line dedicated to the employment of a predoctoral researcher:

- **Title:** Solar array to high voltage power bus: power conversion techniques

  Reference: 4000136441/21/NL/GLC/my

  Funding Entity 1 | Amount: European Space Agency | 67.000€

  Funding Entity 2 | Amount: Miguel Hernández University of Elche | 67.000€

  Duration: 3 years and 1 month

  Period: 01/03/2022 – 31/03/2025

Also, different grants were granted to cover different expenses during the research stay:

- **Title:** Ayudas y bolsas de viaje para la formación y la difusión de resultados de investigación en el marco del programa de doctorado en tecnologías industriales y de telecomunicación, curso 2023/2024

  Reference: Rectoral Resolution 01472/2024

  Funding Entity | Amount: Miguel Hernández University of Elche | 500€

  Period: 01/09/2023 – 31/12/2024

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Chapter 1

"The progressive development of man
is vitally dependent on invention."
- Nikola Tesla -

Introduction

1.1 Motivation

As the effects of climate change become more evident and severe with each passing year, new ways of generating electricity without emitting CO_2 are needed. Space-based Solar Power (SBSP) are large structures located in orbit with the main objective of collecting the solar energy, convert it to electricity, and transmit the energy to a ground station connected to the electrical grid. Although this concept has been studied since the late 1970s, it has not reached a high level of development due to technical limitations and high implementation costs. However, in the past decade, various initiatives from different countries such as Europe [1], United States [2], China [3], and Japan [4] have emerged. The European initiative, SOLARIS, has been promoted by the European Space Agency (ESA). This program aims to lay the groundwork for an orbital demonstrator with power generation capabilities in the order of MW by 2030 and a commercial-scale SBSP capable of generating power in the order of GW by 2040. In comparison, the International Space Station (ISS), with the largest solar-based power system, has only about 200 kW of installed photovoltaic power [5].

The main method for collecting solar energy involves the use of solar arrays, which converts the energy into electricity that is then distributed to the transmitters and other subsystems of the platform. Currently, the European Cooperation for Space Standardization (ECSS) defines a maximum regulated distribution bus voltage of 120 V, as stated in the standard ECSS-E-ST-20C Rev2., clause 5.7.2.g [6]. Scaling up the power beyond tens of kW significantly impacts the electrical distribution by increasing the mass and losses of the harness, connectors and electrical components. Higher distribution bus voltages beyond

100 V must be considered to overcome these drawbacks. An initial approach for a SBSP technological demonstrator, by extrapolating the voltage range for higher power levels defined in the standard at clause 5.7.2.g [6], would require a bus voltage of 900 V, while the commercial-scale version would require a minimum bus voltage of 20 kV.

Additionally, in large satellite power systems bus regulated architectures are common and the output impedance mask is imposed by the same standard in clause 5.7.2.o [6], as shown in Figure 1.

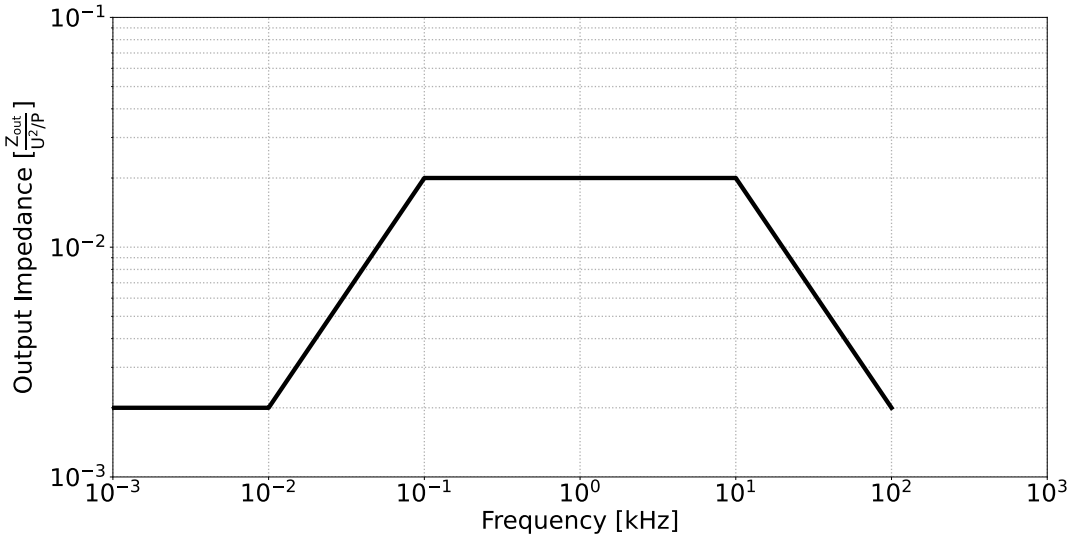

Figure 1. Output impedance mask for a fully regulated bus. Adapted from [1].

The importance of adhering to the output impedance mask lies in ensuring a stable and predictable behaviour for the distribution bus. Specifically, it ensures that the voltage does not exceed 1% of the nominal value during transients loads up to 50% of the power capabilities, as specified in clause 5.7.2.i [6]. However, meeting this mask impedance requirement in High Voltage (HV) systems, i.e. more than 100 V, is a challenge that requires a lot of attention [7].

In space power systems, two types of Solar Array Regulator (SAR) exist, Direct Energy Transfer (DET), where the bus voltage is the same as the output voltage of the solar array, and Maximum Power Point Tracker (MPPT), which adjusts the output voltage of the solar array to obtain the maximum power under varying conditions and then converts it with a DC/DC converter to the designed bus voltage. While the MPPT can deliver higher power levels compared to DET architectures, the overall efficiency can be lower due to the increased number of circuits and converters [8].

A widely adopted DET architecture for regulated distribution bus is the Sequential Switching Shunt Regulator (S3R) [9]. The architecture, as shown in Figure 2, consists of multiple Solar Array Sections (SAS) connected in parallel to the main bus (V_{BUS}) through the DET regulator. The Battery Discharge Regulator (BDR) and Battery Charge Regulator (BCR) are used to supply power to the main bus when there is a lack of solar power and to recharge the battery when needed. The Main Error Amplifier (MEA) is responsible for regulating the bus voltage, and the bus power is distributed through the Power Distribution Unit (PDU).

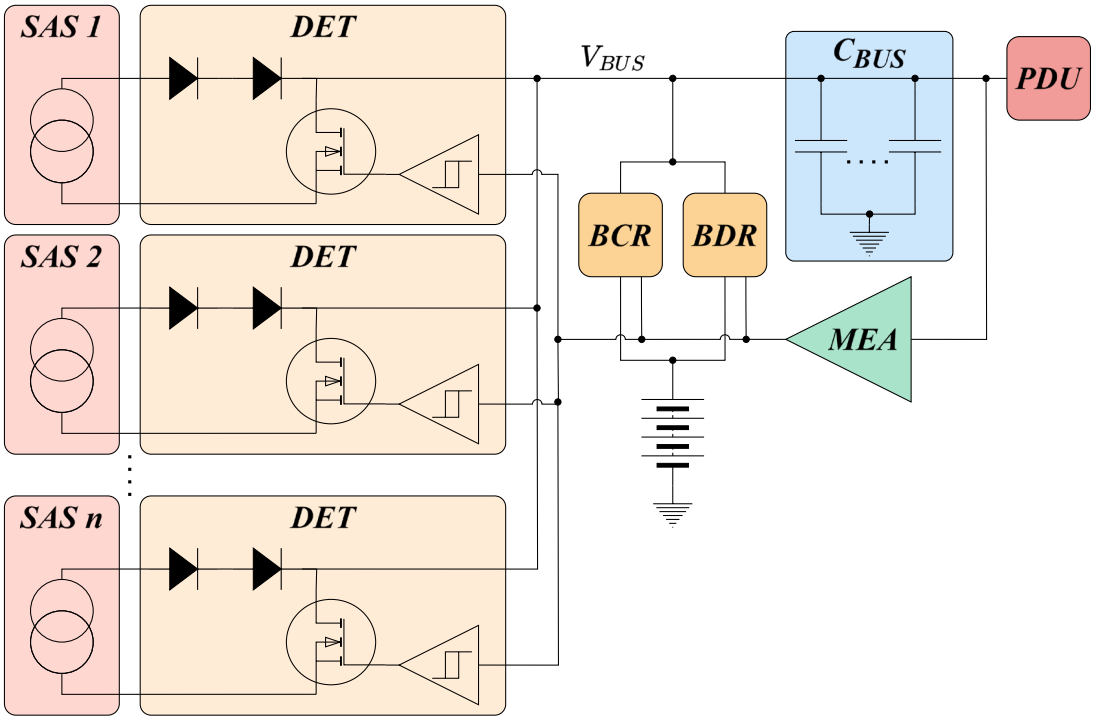

Figure 2. S3R regulated bus architecture

In order to adapt the S3R regulated bus architecture to HV systems, HV solar arrays are needed. Apart from economic aspects, increasing the voltage of the solar arrays is challenging due to many technical issues: arcing between solar cells, electric isolation and arc mitigation in slip rings, string voltage equalization between solar cells, and the reduction of large parasitic elements that impact the design of the distribution system [10], [11], [12].

Different proposals that utilise HV solar arrays for Solar Power Satellite (SPS) or direct drive for electric propulsion are presented in Table 1.

Table 1. Proposals and technological demonstrators of high voltage solar arrays

Application	Voltage	Reference
Solar Power Satellite	500 V	[13]
Solar Power Satellite	400-500 V	[14]
Direct drive electric propulsion	300 V	[15]
Direct drive electric propulsion	300 V	[16]
Arc mitigation technology demonstrator	350 V	[10], [11]

A possible solution to avoid the use of HV solar arrays and maintain existing 100 V solar arrays is to integrate a step-up voltage converter that adjust the desired distribution bus voltage. For SBSP systems, the implemented architecture must be scalable in power to facilitate easy implementation and ensure an overall high efficiency of the distribution system.

Based on the exposed points, the main motivation of this doctoral thesis is the development and validation of a novel architecture concept that provides power conditioning from Low Voltage (LV), <100V, solar arrays to a HV distribution bus according to space power requirements, i.e. ECSS standards.

1.2 Subject addressed

Throughout this thesis, various concepts will recur that are integral to the subject addressed. Depending on the context, these concepts may have different meanings. To provide a baseline for the reader, the main relevant concepts are defined as follows:

- **Space-based solar power:** This type of spacecraft, also referred in the literature as solar satellites for simplicity, is a concept aimed at generating vast amounts of power, in the order of GW, by harnessing the energy of the Sun. One of the most studied methods involves using large photovoltaic solar arrays to convert solar energy into electricity, which is then transmitted to a ground station on the surface of Earth via microwave or laser transmission. Another method proposed the use of optical reflectors to concentrate solar light onto conventional solar

plants, thereby increasing power production even at times of low solar irradiance, such as dusk and dawn. However, to transmit a high power beam to the Earth's surface could have undesired side effects on the environment, atmosphere, local infrastructure and human health. These potential impacts, along with methods to mitigate or reduce them, must be thoroughly studied before the implementation of solar satellites.

- **Power conditioning and distribution unit:** The system responsible for conditioning the voltage of the solar arrays, managing the charge and discharges of the batteries, and distributing power to the main bus for the rest of the spacecraft's system is the Power Conditioning and Distribution Unit (PCDU). Different architectures can be implemented depending on the requirements of the spacecraft, primarily divided into unregulated and regulated bus voltage. For regulated buses, the voltages are standardized according to the ECSS based on the maximum power, with standard voltages being 28 V, 50 V, 100 V and 120 V.

- **High voltage:** In space applications, when the electric potential, whether Direct Current (DC) or Alternate Current (AC), between two points is high enough for a given atmospheric pressure and distance, effects such as partial discharge, corona or arcing can occur. These effects occur in an air medium at a minimum voltage of 330 V and a pressure per distance of 7,3 mbar·mm, according to the Paschen law. During the design phase, it must be considered the conditions for these effects and to implement mitigation methods. Such methods include avoiding operation in partial pressure conditions or introducing isolation layers, such as potting, between the electric potential.

- **DC/DC power converter:** Power converters take the voltage and/or current at the input, and their electrical parameters are modified and adapted at the output. Generally, solar arrays, batteries and electric loads are powered by direct current, so DC/DC power converters are commonly used in space applications. One type of DC/DC converters are the DC transformer (DCX). This converter achieves a constant conversion gain and galvanic isolation using a transformer. Since DC power cannot be directly transferred through a transformer, one method to generate alternating current is by generating a resonance between an

inductor and a capacitor, which minimise switching losses and Electromagnetic Interferences (EMI) emissions.

- **Analog control loop:** Control and adaption of the voltage and power of the distribution bus are performed using a voltage feedback loop. Typically, a main error amplifier is employed, where the output voltage is measured and compared to a stable reference voltage. This amplifier generates an error signal that controls the DC/DC power converters. In general terms, analog control is considered to be the process of regulating a system without the utilisation of programmable digital electronic circuitry.

- **Modularity:** One of the main ideas for achieving a high power, high voltage distribution bus involves the use of large number of solar array sections at a given voltage, which are then converted to high voltage. In reliability terms, the use of a single module is not feasible; hence, DC/DC power converters must be capable of connecting their outputs in both parallel and series configuration. This should be accomplished while maintaining a simple design.

1.3 Objectives

The main objective of the PhD thesis is to develop, implement and validate a novel architecture for high power and high voltage space platforms, such as SBSP. The core concept involves integrating two well-established techniques used in the European space sector into a single module. This module will convert and regulate the low voltage from the solar arrays to a high voltage distribution bus. A highly modular system is to be designed, and each module can interconnect with other modules in various configurations, achieving the desired output voltage regardless of the voltage or current from the solar arrays.

1.3.1 Specific objectives

The specific objectives of this PhD thesis were established in a research agreement with the European Space Agency, where contract details are included in section 1.4.1. The specific objectives are listed as follows:

1. **Bibliography review and study** of the technology and development plans of solar satellites, the architectures used in spacecraft for power conversion and distribution, and the power conversion techniques for high voltage output.

2. **Establish the requirements for power semiconductor requirements and review the market** to study the availability and suitability of those components for use in space environments.

3. **Conduct a formal analysis of the proposed architecture,** detailing the working principles of the converter, regulation, and loop control. Evaluate the suitability of the proposed DCX converter as a solar array regulator.

4. **Establish a design methodology** for the proposed architecture in compliance of the requirements established by the ECSS-E-ST-20C-Rev.2 [6].

5. **Development of a prototype** with different modules and representative of existing systems.

6. **Development of a testbench** to perform tests and validation of the proposed architecture at the *Space Power & Electronic Systems* (SPES) research group laboratories, located in the Torrevaillo building at the Miguel Hernández University of Elche (UMH).

7. **Validation of the architecture (TRL 4)** using the prototype implemented and the testbench developed in the SPES laboratories of the UMH.

8. **Study the electric isolation** of the components most susceptible to high voltage effects in vacuum and partial pressures conditions at the facilities of the *European Space Research and Technology Centre* (ESTEC) of ESA.

9. **Analysis of results** of the different tests and validations of the developed architecture, including the data obtained from the electric isolation test campaign.

10. **Produce scientific papers** for high-impact and open-access journals to disseminate the ideas and results obtained to the scientific community. Additionally, research findings are presented at relevant international and national conferences within the research field.

1.4 Thesis framework

1.4.1 Projects

This thesis is part of the research project entitled "Solar Array to High Voltage Power Bus: Power Conversion Techniques" partially funded by the European Space Agency and the University Miguel Hernández of Elche, with the reference number 4000136441/21/NL/GLC/my. The research was conducted by the group *Space Power & Electronic Systems* at the Miguel Hernández University of Elche and headed by Prof. Ausiàs Garrigós.

The main objective of the project is to study, design and validate efficient high voltage photovoltaic power conversion for solar power satellites and to evaluate its potential benefits for current satellite power systems.

1.5 Equipment and Methodology

1.5.1 Equipment

The most relevant equipment used for the development, test and validation of the project are listed below.

- *Space Power & Electronics Systems* – University Miguel Hernández of Elche
    - Solar array simulator Agilent E4351B
    - Oscilloscope Tektronix MSO46
    - Oscilloscope Tektronix DPO-4034
    - Multimeter Fluke 8846A
    - Vector network analyzer OmicronLab Bode100
    - Power analyzer Yokogawa WT1800
    - Thermographic camera FLUKE Ti450

- Digital control board SPCard

- *High Voltage laboratories* TEC-EP – ESTEC ESA
  - Solar array simulator Agilent E4360A
  - DC electronic load Chroma 63630-600-15
  - Pressure sensor Pfeiffer PKR 251
  - High voltage vacuum chamber.
  - Non-destructive insulation tester JP 30A

1.5.2 Methodology

The methodology employed to conduct the research for this thesis is presented below:

- **Electronic design:** Discrete components and analog integrated circuits are used to create the necessary subsystems. Each electronic subsystem consists of different functional blocks interconnected to form a complete and complex system.

- **Simulation:** LTspice and PSIM simulation tools are employed to analyse the working principle of the proposed designs. This step is important for preliminary verification of the functionality before physical implementation. During experimental testing and validation, simulation tools are used to replicate unusual behaviour and facilitate a better understanding.

- **Hardware design:** After defining the schematics of the electronic circuits, a Printed Circuit Board (PCB) is designed and manufactured. Factors such as control signal integrity, power dissipation, adaptability and ease of signal measurement are considered during the design phase.

- **Assembly and soldering:** The PCB is manufactured externally by a specialized company. The mechanical and electronic components are then assembled and soldered in-house. Power transformers are wound and prepared by hand.

- **Experimental validation:** Each functional block is individually tested to ensure proper operation. The complete system is then validated under laboratory conditions using available equipment (listed in section 1.5.1). The architecture is tested in various configurations within a range of input voltage and current levels. During this phase, changes are made to the circuit to fine-tune its performance and achieve the desired functionality. Additionally, the main part of the architecture is tested and validated under vacuum and partial pressure conditions to evaluate electrical isolation.

- **Analysis of results:** Each experiment performed is thoroughly documented. The data collected is analysed and the results are verified to ensure that they meet the defined requirements.

- **Scientific papers:** The context, methodology, design, experimental results, and other relevant scientific knowledge are documented in scientific papers. This ensures that the work can be easily accessed by the scientific community.

- **Conferences:** Apart of scientific papers, participation in international and national conferences facilitates the exchange of ideas with other scientists, generating a discussion aimed at further improving each other works.

1.5.3 Thesis structure

As previously mentioned, the PhD thesis is presented as a compendium of published articles, which are incorporated into the main core of the document.

The thesis is divided in four main blocks listed below:

- **Introduction:** Context and state of the art.
- **Thesis Core:** Scientific journal publications.
- **Closure:** Conclusion and future lines of research.
- **Annex:** Circuit schematics, experimental setup, semiconductors evaluated, and software code.

Chapter 2

Context & state of the art

2.1 Introduction to electrical power system

All spacecraft require electrical energy to power their subsystems, and four key questions must be addressed during the design process: how power is generated (power generation), how power is stored (power storage), how it is conditioned between the different subsystems (PCU) and how power is distributed to the loads (PDU). These four blocks together are defined as the spacecraft's Electrical Power System (EPS). The most common solution combines photovoltaic power generation with batteries for energy storage [17], as illustrated in Figure 3. This configuration provides the basis for the discussion and implementation of this work. In particular, this thesis focuses on PCU for a particular type of spacecraft.

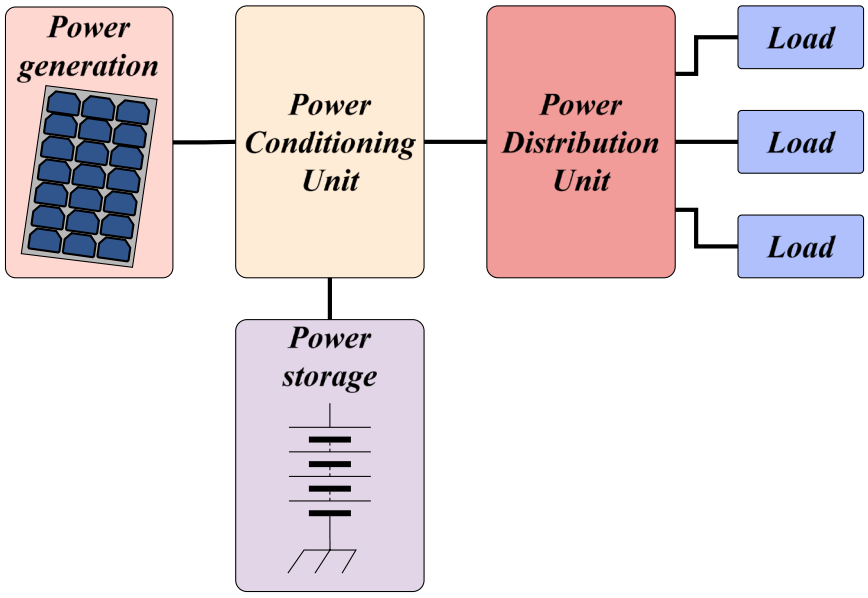

Figure 3. Generic diagram of the EPS in a photovoltaic-battery configuration.

The PCU can be configured within a range of architectures, adapted to the specific requirements of the spacecraft, including, among others, energy demand, variations in energy generation due to changing environmental conditions, voltage distribution bus stability, and

design complexity. The classification of these architectures is based on the type of distribution bus used, unregulated or regulated.

The most common unregulated bus architecture connects the battery directly to the main bus, which causes the bus voltage to vary according to the state of charge of the battery. The photovoltaic generator is connected to the unregulated bus in one of two ways: using a DET regulator or using a DC/DC converter with a MPPT. DET architectures are the simplest, but they have a key disadvantage: the voltage at which the SAS operates is fixed by the battery voltage, which results in reduced performance in most cases. To solve this problem, it is necessary to integrate a DC/DC converter with a MPPT, which will ensure that the maximum power is delivered during operation [18]. Figure 4 shows a typical implementation for both unregulated architectures.

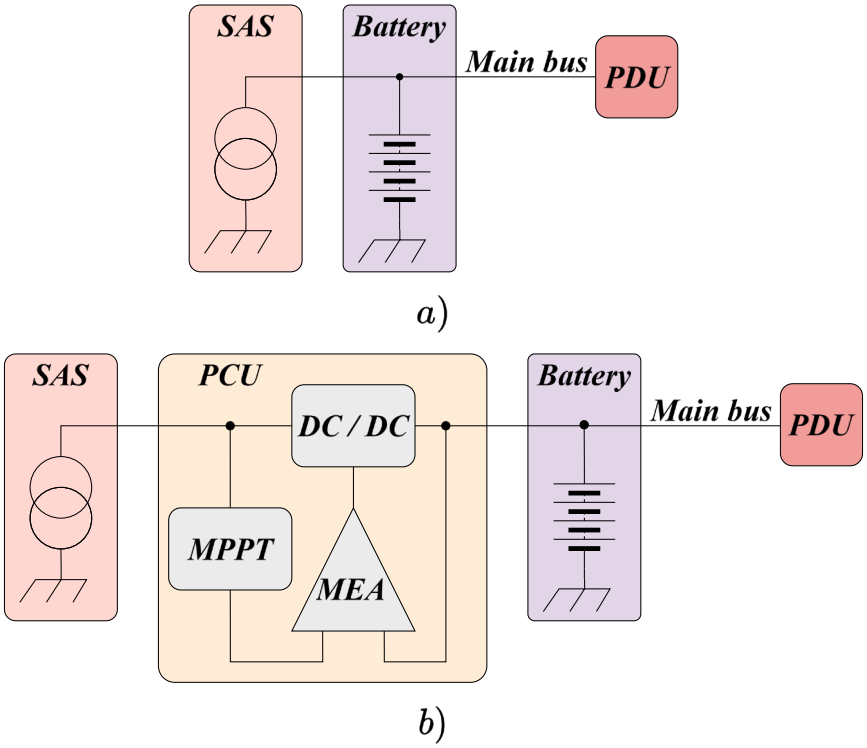

Figure 4. Simplified unregulated architecture.
a) DET b) DC/DC MPPT.

The use of MPPT unregulated bus architectures is typically found in missions where the temperature and irradiance of the SAS experience significant fluctuations over time. This includes satellites operating in Low Earth Orbit (LEO), interplanetary missions, or any scenario where the voltage-to-current curve of the solar array exhibits large variations throughout the mission.

In regulated bus architectures, the battery is connected to the bus via a BDR to maintain a constant bus voltage. Again, regulated architectures accept DET and MPPT solar array regulators. DET architectures are the most common in large telecom satellites, although the MPPT bus regulated has been used in some European scientific missions, such as Mars Express, Rosetta and Venus Express [19].

In DET bus regulated architectures, a common method for bus voltage regulation involves hysteresis and sequential ON-OFF control of the SAS. This DET control method is known as S3R [9], [20]. An evolution of this architecture is the S4R [21], [22]. In the S4R, unused SA sections are connected directly to the battery for charging. Figure 5 illustrates a general implementation of the S3R and S4R topologies.

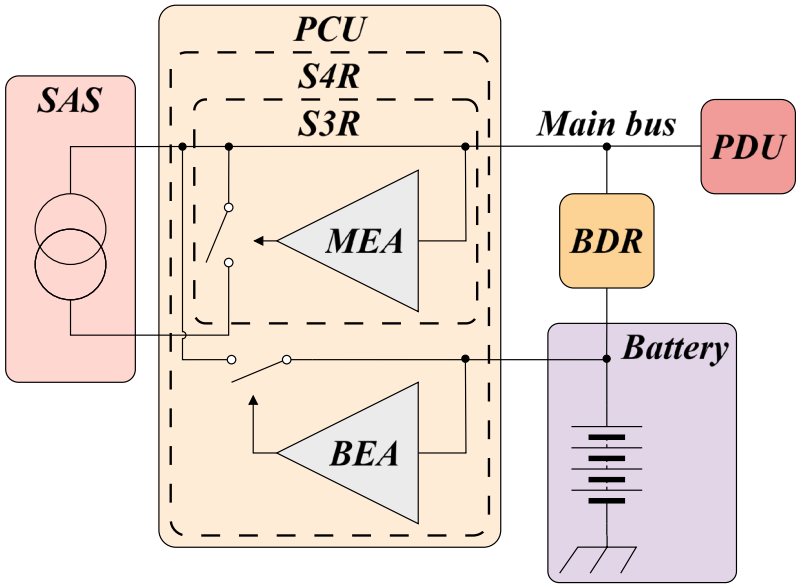

Figure 5. General diagram of a regulated-DET bus based on a S3R/S4R.

DET regulated bus architectures are particularly suitable for missions in which solar irradiance and temperature remain stable over time, such as telecom satellites operating in Geostationary Earth Orbit (GEO). Under such conditions, the SAS can be sized to operate close to its maximum power point, thus eliminating the need for an MPPT.

2.2 High voltage in spacecraft power systems

In terrestrial applications, 1.500 V is the limit for LV-DC power systems [23]. However, in space applications, the definition of HV is based on the breakdown voltage of the surrounding insulating materials, which can result in adverse effects such as partial discharges, corona, or arcing. Therefore, the voltage can be lower than 1.500 V. The safety-voltage threshold depends on the spacecraft's environmental conditions, being the composition and pressure of the atmospheric ambient the primary factor. The electrical breakdown in a gaseous material is guaranteed to occur at a certain voltage when the relationship between the gas pressure and the distance between the electrical potential is fulfilled, as defined by the Paschen's law. The voltage at which the electrical breakdown occurs is not constant; this can be represented as a Paschen curve as shown in Figure 6, under various gas and pressure conditions.

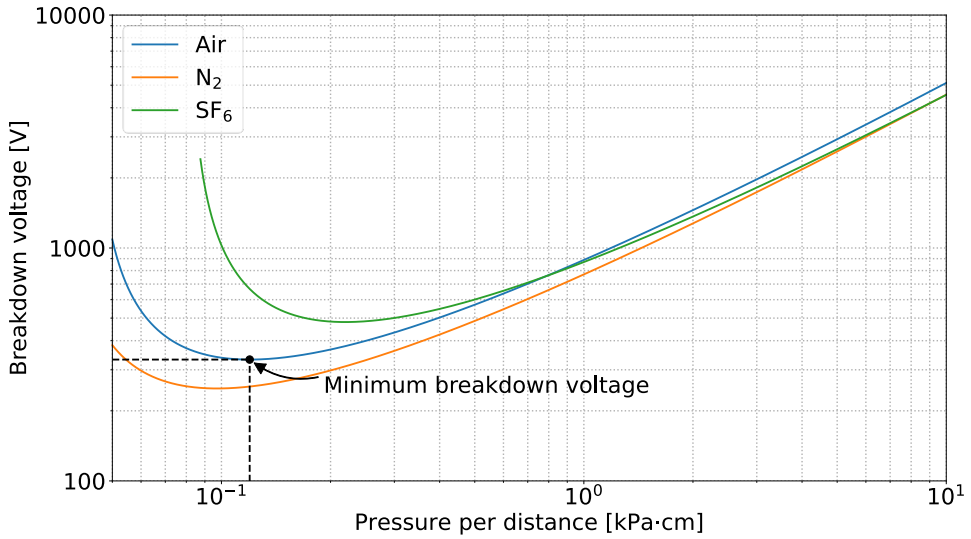

Figure 6. Paschen curve for air, N_2 and SF_6. Adapted from [24].

In general, for spacecraft in Earth's orbit, the minimum air breakdown voltage occurs at 330 V for a pressure-distance ratio of 7,3 kPa·cm [25]. However, these values are subject to variations due to factors such as temperature fluctuations [26], voltage slew rate [27] or differences in the material composition of the electrical charged parts [24]. Consequently, the European space standards stipulate that, for most applications, systems exceeding 200 V are considered HV [25].

During the Launch and Early Operation Phase (LEOP), if the interior of the spacecraft is not pressurised, atmospheric air will gradually escape, causing a depressurisation over time until the vacuum of space is reached. The duration of this process is based on the size of the spacecraft and the system module structure, which can vary from several hours to several weeks. Achieving a high vacuum condition (10^{-4} mbar or lower) ensures that the spacecraft environment reliably functions as an electrical insulator [25], [28].

2.2.1 Hazardous effects

A partial pressure condition may arise in a spacecraft under various scenarios, including depressurization during LEOP, gas leakage from a pressurised vessel, outgassing of on-board components or by space debris. These conditions can cause dangerous effects that can interfere with or damage the spacecraft subsystems. The mechanism of electrical discharges in gases has been widely documented in the literature [29], and the resulting effects depend on the voltage applied and the current flow through the medium, as illustrated in Figure 7.

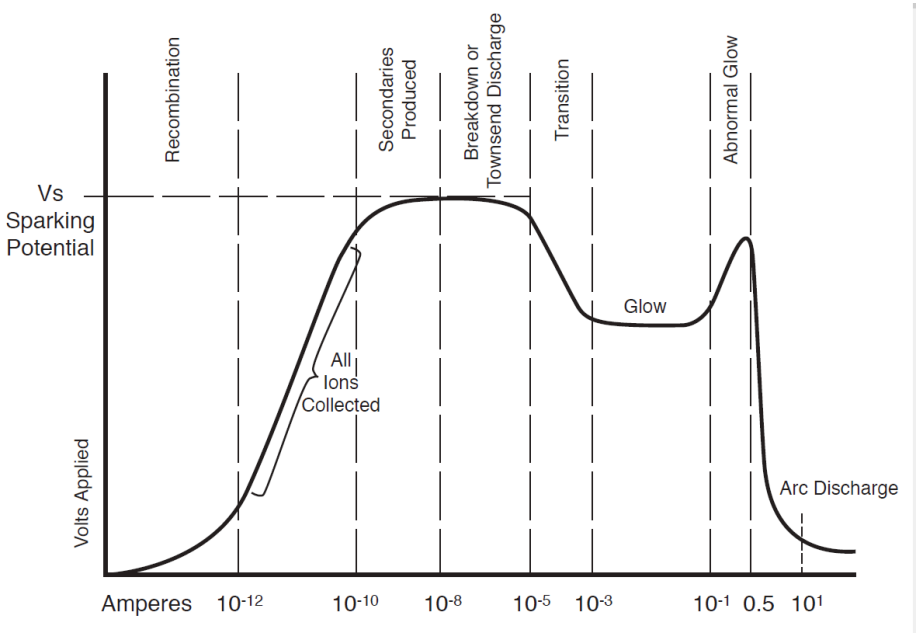

Figure 7. Gas discharge characteristic. Extracted from [28].

When a constant voltage is applied between two terminals under constant low-pressure gas conditions, as the voltage increases but remains below the breakdown threshold, ions begin to accumulate between the anode and cathode due to the acceleration of electrons. This process results in a very small current, in the order of pA. At this stage, the medium

retains its insulation; however, as the voltage approaches the breakdown threshold, a critical point is reached at which the accumulated ions trigger a cascade of electrons between the anode and the cathode, forming a conductive path. This phenomenon is known as the Townsend discharge. Beyond this point, the ionised gas of the cathode emits a visible glow in a process called corona effect or corona discharge, as depicted in Figure 8.

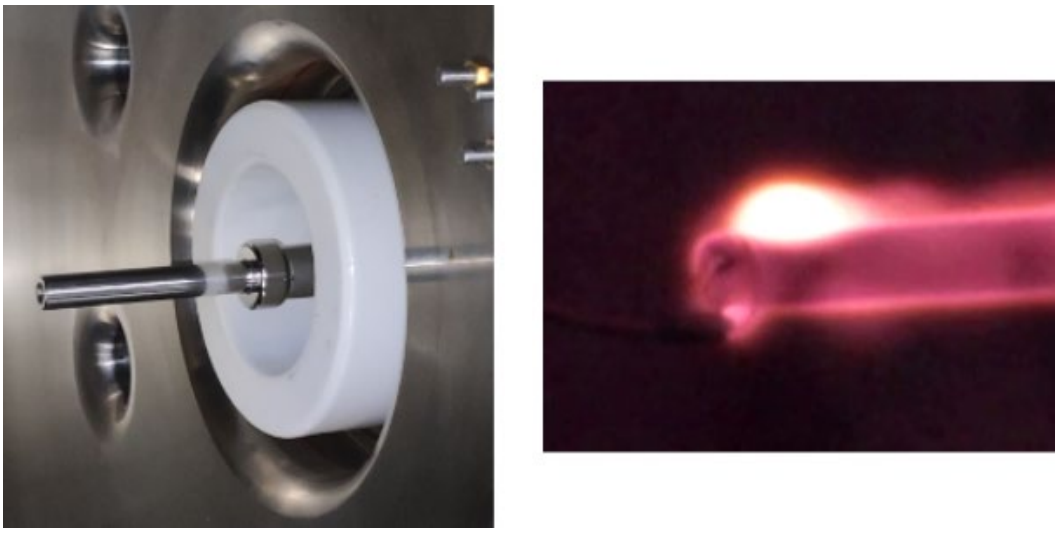

Figure 8. Left: Cathode connector from a vacuum chamber Right: Corona effect on the cathode at 600 Vdc.

The corona effect results in a leakage current, in the order of mA. If the voltage is sustained, the corona expands, leading to the closure of the conductive path between the anode and cathode. This results in a full electric arc discharge, effectively creating a short circuit between both terminals, as shown in Figure 9. Furthermore, it is important to note that both effects are a significant source of EMI emissions, which can have a substantial impact on some payloads or other subsystems that are susceptible to noise.

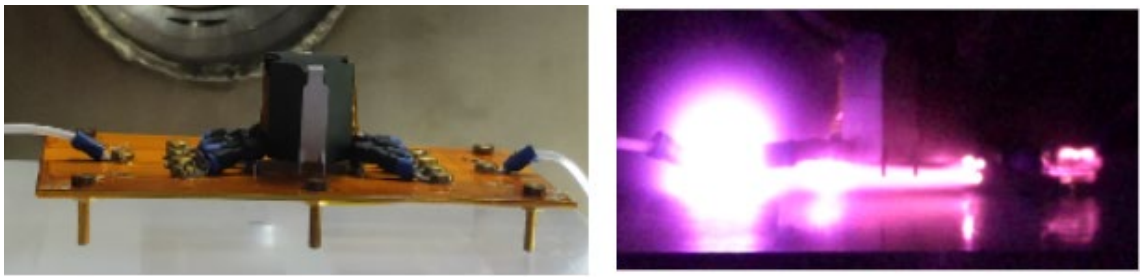

Figure 9. Left side: Transformer under test. Right side: Electric arc between the transformer's terminal at 600 Vdc. Partially extracted from [30].

Due to imperfections in the manufacturing process, solid insulators contain trapped gas bubbles [28]. When the conditions inside these bubbles fulfil the conditions defined by Paschen's law, a partial discharge becomes possible. This phenomenon is a repetitive process in which the gas bubble behaves as a capacitor. Initially, the bubble begins to charge under the HV electric field. As the voltage across the bubble increases and reaches the voltage breakdown threshold, the stored energy is suddenly released. Repeated partial discharge gradually degrades the solid insulator, potentially resulting in a total failure in the long term [25]. An equivalent circuit schematic illustrating the partial discharge is shown in Figure 10.

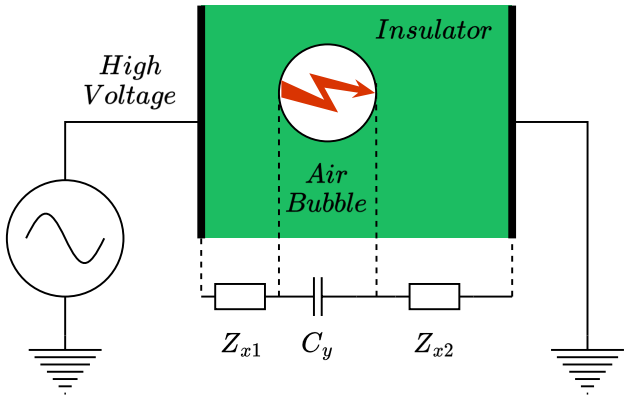

Figure 10. Equivalent circuit schematic of a partial discharge on a trapped air bubble.

In order to ensure the proper operation of HV systems aboard spacecraft, various strategies can be employed to either mitigate or avoid the hazardous effects. The first option is to incorporate a solid insulator, composed of epoxy or silicone materials, into the HV components in a process known as potting. This approach provides robust protection across a wide voltage range, enabling HV operation during LEOP and offering an additional safeguard against contamination [28]. However, it should be noted that this is a heavy mass solution and typically exhibits low thermal conductivity but can be enhanced by incorporating filler material such as silica [25]. It is also crucial to minimise air bubbles and contaminants during the manufacturing process to reduce the possibility of partial discharges.

The second option involves the use of a layer of solid insulator as a conforming coating on the electronic components. Suitable for voltages up to 3 kV, this layer is typically made of polymers or silicones. In comparison with potting, this method has a reduced mass impact and offers improved thermal conductivity. However, it is not recommended to power up the HV components during LEOP, as a large electric field is still present on the surface of the

coating, which can induce corona effects [28]. It is also important to note that both options require extended time to degas, which can induce partial pressure issues in unprotected HV components.

The third approach makes use of the high insulation properties of vacuum without applying additional insulation to HV components. This method reduces mass and does not interfere with thermal management systems. Nevertheless, it is important to note that the HV subsystem is still fully exposed to the environmental conditions, including partial pressures conditions that may be generated. Consequently, the system cannot be powered up during LEOP [25]. Vent holes can be incorporated into the shielding to reduce the degassing period. On the other hand, a high degassing material, such as plastics or polymer coatings, should be avoided [28].

In summary, a combination of different insulation strategies is employed by manufacturers of HV space systems. For instance, Figure 11 shows a Travelling Wave Tube Amplifier (TWTA) Electronic Power Conditioner (EPC) developed by ASP. In this module, the HV components are fully potted to ensure robust insulation, while the ancillary circuits are protected by a conformal coating as an insulation layer. The combination of these techniques allows for mass optimisation.

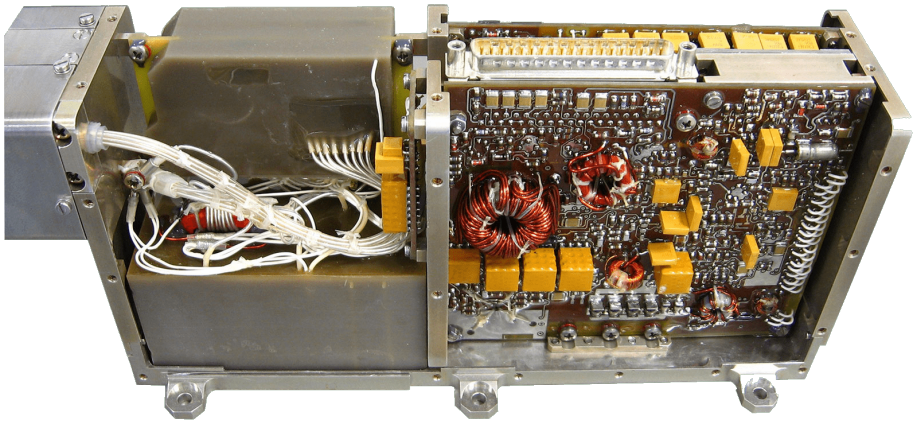

Figure 11. 7 kV TWTA EPC from ASP. Extracted from [31].

2.2.2 Applications and development challenges

HV systems have historically had several applications in space vehicles, including electric propulsion systems, TWTA, and scientific payloads. In addition, they are now considered essential for increasing platform power in large satellites, space stations and SBSP satellites. These systems require HV buses to efficiently manage the distribution and power transmission.

The development of HV electronic circuits poses significant technical challenges, from the selection of components to the design of PCBs to ensure reliability over extended missions [32]. In addition to addressing the HV hazardous effects, such as corona effects or arc discharges, as discussed in section 2.2.1, radiation exposure becomes a critical consideration. The impact of high-energy particles affects all electronic parts, particularly the power semiconductor components, making them susceptible to Single Event Effects (SEE). SEE can result in temporary loss of functionality, component degradation or even component destruction from a Single Event Breakdown (SEB). The probability of such events is heavily dependent on the operating voltage, and derating is required as stated in the European standard ECSS-Q-ST-30-11C [33]. Consequently, the selection of power semiconductors for HV applications is critical and constrained by their reliability [34]. These aspects are discussed in more detail in section 4.4.1.

2.2.2.1 High power distribution buses

The ESA standard for electrical and electronic space engineering, ECSS-E-ST-20C [6], specifies a maximum regulated distribution bus voltage of 120 V for a power bus of approximately 20 kW. To date, the ISS is the spacecraft with the largest power generation capacity in space, with 105 kW as maximum output through a 120 V distribution bus [5]. In comparison, the Tiangong Space Station, developed by China, provides 27 kW with a 100 V distribution bus voltage [35]. The orbital Lunar space station, Lunar Gateway, is currently under development through a collaborative effort involving the space agencies of the United States of America, Europe, Japan, Canada and the United Arab Emirates [36]. The Lunar Gateway is expected to operate with a 120 V distribution bus and deliver a maximum power of 32 kW [37]. This power and voltage range is very similar of large telecommunication

satellites, such as the Eurostar NEO platform, designed to generate between 13 and 30 kW [38]. Furthermore, larger power systems are anticipated for other future applications such as Lunar or Martian surface bases [39]. In [40], a lunar base with an initial power capacity of 1 kW and a scalable capacity up to 100 kW is envisioned. Given the possibility that the modules can be separated by kilometres, distribution and transportation buses operating at 120 V, 600 V and 1.000 V would be required [39], [40].

Maintaining a 100 V distribution bus for a power consumption of over 20 kW results in heavy and bulky systems, and complicates voltage regulation due to large bus currents, requiring a very low output impedance [6]. The low output impedance constraint impacts the size of the bus capacitor, wiring and connectors, complicating the design of the EPS. Conversely, adopting higher distribution voltages, e.g. 300V as proposed in [12], [41], reduces system mass and power losses while enabling the implementation of new and simpler architectures [16].

In DET architectures, the SAS voltage is the bus voltage, meaning that DET-based HV distribution would require HV-SAS. This introduces a significant risk of hazardous HV effects, such as electrical discharges in the SAS. At the triple junction point where the vacuum, conductor and dielectric meet, combined with plasma accumulation, the likelihood of an electric arc is increased. When the solar array accumulates an electric field of -200 V or lower, an electric discharge is generated, which degrades the solar cells over time [42]. In order to understand and mitigate this phenomenon, several experiments have been conducted under laboratory conditions [12], [43]. To advance the development of HV-SAS, two in-orbit experiments, HORYU-II [10] and HORYU-IV [11], have been launched. Typical satellite solar cells, with an added insulator to minimise the high electric field concentration, were tested in these experiments. Optical cameras and current sensors were used to measure the occurrence of partial discharges, providing valuable data for the design of HV-SAS.

Slip rings used in Solar Array Drive Mechanisms (SADM) are also critical components sensitive to HV operation. One approach to mitigate the risk of HV effects is to enclose the slip ring within a sealed container, kept at high vacuum or filled with dry air at 1 bar [12]. While this method reduces the likelihood of discharges, the mechanical interface remains a potential source of leakage. Alternatively, arc mitigation techniques can be incorporated directly on the slip rings. A simple and effective method is to use a resistor divider between

the high-side and low-side of the slip rings. This configuration acts as a partial Faraday cage, increasing the minimum voltage breakdown threshold from 400 V to 600 V [44].

2.2.2.2 Electric propulsion

Electric propulsion systems are becoming the preferred choice for spacecraft in a wide range of missions due to their ability to deliver high thrust and achieve significant speeds with low mass compared to chemical propulsion systems [45]. Among the various types of electric thruster available, the Hall Effect Thruster (HET) is commonly used in medium and large spacecraft. It works by accelerating an ionised propellant, typically xenon gas, using the force generated by an electric field. Despite the low force applied to the spacecraft, it provides high efficiency and sustained propulsion, making it well suited for orbital raising, station keeping or deep-space exploration.

The Power Processing Unit (PPU) is used to power the different elements of the HET, as represented in the simplified schematic in Figure 12. The typical voltage requirements for each element are as follows: 40 V for the magnet supply, 20 V for the cathode heater, which is switched off after the start-up sequence, 35 V for the keeper supply, and 300 V to 600 V for the anode or discharge supply [46].

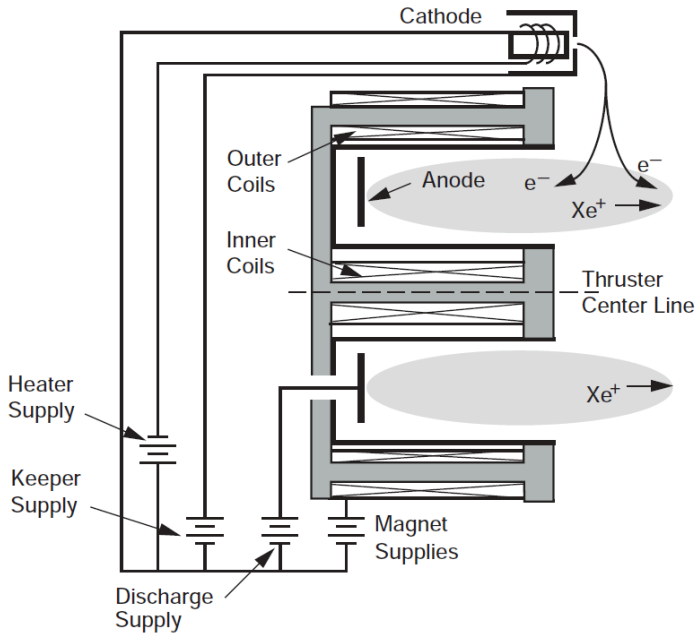

Figure 12. Electrical schematic of a HET. Extracted from [45].

Due to the HV of HET propulsion systems, different studies have proposed the use of HV-SAS directly connected to the HET without any kind of power converter. This configuration is known as direct drive architecture and simplifies the PPU design [16]. Depending on the bus topology, there are different direct drive architectures, including voltage regulation based on S3R or MPPT [47]. An alternative to HV-SAS involves the use of an isolated DC/DC converter to step up the voltage from a LV-SAS to the HET, as shown in Figure 13. This architecture can also power other payloads when the thruster is inactive.

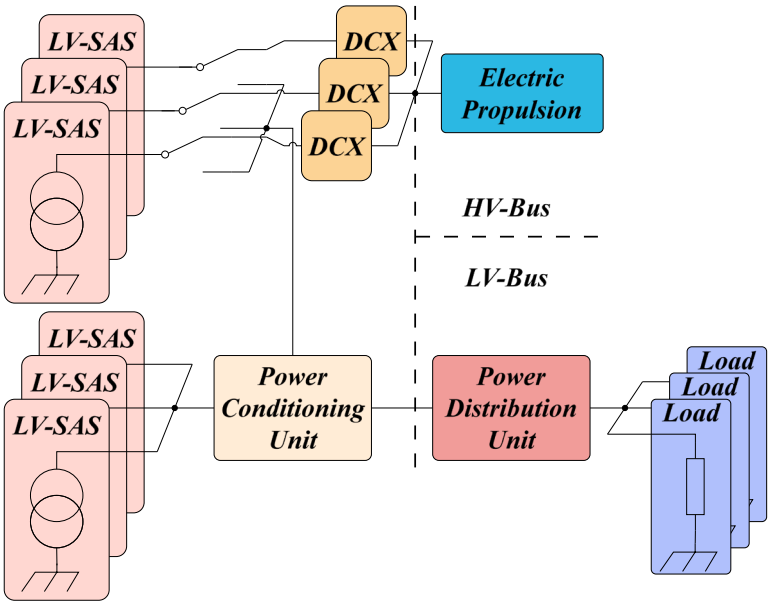

Figure 13. Direct drive architecture with isolated DCX. Adapted from [47].

2.2.2.3 Payloads

Telecommunications satellites are equipped with TWTAs, which are used to amplify a radiofrequency (RF) signal to power levels ranging from 200 W to 1,5 kW by incorporating an HV-DC bias supplied by the EPC. Large satellites often require multiple TWTAs for each RF band, increasing the satellite's overall mass, volume and power demand. For example, the Ka-Band amplifier used in a software-defined radio implemented for the ISS uses a 7 kV EPC from a 35 V unregulated bus [48]. A similar requirement is seen in a Q-band TWTA, which demands a 15 kV EPC to deliver a maximum output power of 266 W [49].

Solid-State Power Amplifiers (SSPA) are being adopted to replace TWTAs, due to their capability to reduce the overall mass and volume of the system by operating at lower voltages

than TWTAs. The voltage range required varies from a maximum of 9 V for a L-Band transceiver [50], up to 36.5 V for a C-Band SSPA [51], below the HV threshold to avoid hazardous effects.

Earth observation satellites carry payloads to facilitate the study of climate, weather and other aspects of our planet. For instance, the *EarthCARE* programme, a joint initiative between ESA and Japan Aerospace Exploration Agency (JAXA), is designed to improve our understanding of clouds and aerosols [52]. The platform uses a high-power cloud profiling radar, requiring a 17 kV EPC for 200 W output power, with potted HV parts for reliability [53]. Scientific missions involving the measurement of plasma, radiation and other types of particles require HV EPCs. Some companies offer adaptable EPCs for such payloads, featuring output voltage ranging from 2 kV to 12 kV and power outputs up to 12 W [54].

2.3 Space-based solar power

SBSP, also known as SPS, is a type of spacecraft designed to capture solar energy and transmit it to stations located in an astronomical object. The concept was first introduced in 1968 [55] and subsequently patented in 1973 [56] by Peter Glaser, who envisioned a GEO satellite. The spacecraft would be equipped with an enormous photovoltaic solar array oriented towards the Sun. This energy would be transmitted to Earth via microwave or other type of wireless power transmission, e. g. laser. A simplified diagram of the SBSP is shown in Figure 14.

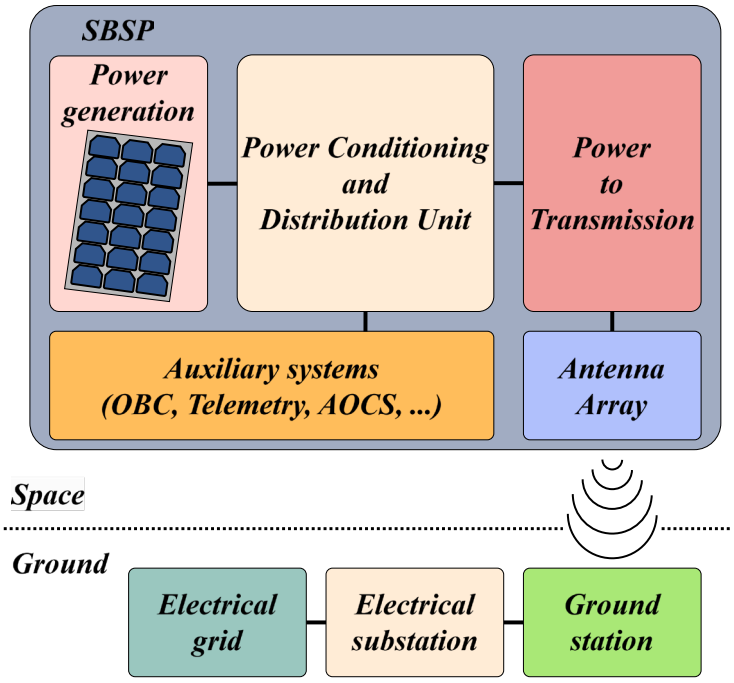

Figure 14. Main system elements of a generic SBSP

2.3.1 System and technical characteristics

The high launch costs and technical complexity of SBSP platforms require them to operate from MW to GW to achieve economic viability. The first proposal by National Aeronautics and Space Administration (NASA), in 1974, estimated the cost of a 5 GW SBSP in approximately $6,5 trillion [57], equivalent to $47,8 trillion when adjusted for current inflation. A recent 2024 study predicts a significantly reduced cost for a 2 GW SBSP platform

by incorporating various technological and manufacturing advances, with a total cost estimate of $276 billion [2].

The deployment of a full-size SBSP system, with an area of over 25 km^2 of solar array [57], requires advancements in several key technologies. These include light and efficient solar cells for power generation, reliable HV power conversion and distribution, and high-power wireless transmission. Precise tracking and directing of the main transmission beam from the transmitter to the receiver is also essential, as is the development of rectifying antennas, also known as rectennas.

Wireless power transmission via microwaves has been a relevant topic of discussion and research for many years [58]. High-power RF signals for power transmission can be generated using devices such as TWTA, magnetrons or klystrons, which produce an unmodulated continuous-wave, narrow-bandwidth signal [56], [59]. Alternatively, SSPA have also been considered for DC to RF power conversion due to their lower voltage operation and size [59], [60].

Most of the studies on wireless power transfer for SBSP have been undertaken under laboratory conditions. However, in March 2023, the first orbital demonstration was conducted with the Microwave Array Power transfer LEO Experiment (MAPLE), a payload onboard the Vigoride-5 satellite [61]. The demonstration used a DC to RF module, operating a SSPA, with a power consumption of 6.85 W, including the power amplifiers and the auxiliary circuitry. The maximum power received at the ground station was 251 mW, giving to an overall efficiency of 3.66 %.

As outlined in section 2.2.2.1, high-power space platforms require HV distribution buses in order to minimise losses and mass, as well as to enable a feasible electrical and control design. However, it should be noted that this approach presents significant challenges, including the risk of HV hazardous effects. Based on the rationale behind the ECSS-E-ST-20C, for 2 GW SBSP, a 32 kV bus voltage would be required [6]. One of the early SBSP proposals considered distribution voltages higher than 40 kV for an 8 GW platform operating in a DET architecture, where SAS shares the same voltage level. In this regard and to ensure reliable operations over a 10-year period, the development of switches and protection devices capable of functioning at 40 kV and 500 A is essential. Extended protection strategies against HV hazardous effects are critical. Furthermore, the distribution

of high current over several kilometres of harness raises concerns about significant magnetic fields, which could interfere with the attitude stability [57].

A recent European study for a 2 GW SBSP proposed a design featuring two independent EPS, each operating with a distribution voltage of 20 kV [14]. In contrast to the previous proposal, which required 20 kV SAS, this design sets the SAS at 400 V, still being considered as HV-SAS. In this study, the bus is regulated via a S3R and transformed into 20 kV within the PCU by dedicated high-power DC/DC converters. While the study acknowledges the availability of power converters rated up to 1,85 kV and 5 kW, it highlights the critical need for substantial technological advancements in power electronics to fulfil the elevated voltage and power demands.

One alternative to space photovoltaic conversion is the use of sunlight reflection and photovoltaic conversion on Earth. This concept offers the potential to generate solar energy at night, to light urban areas to increase daylight, or to light farmland at night to increase crop production [62]. Another study, based on the same concept, explored a constellation of 3.987 reflectors positioned in LEO to achieve a maximum 5,6 GW power generation. This projection assumes a photovoltaic Earth plant of 50 km^2 [63].

Regardless of the method employed for power transmission, whether by microwave waves, lasers or reflecting sunlight, the concentration of high energy in a specific area raises concerns about potential effects on human and environmental health. This aspect, in conjunction with other issues, has generated some scientific controversy [64]. The European Union, in directive 2013/35/EU [65], established a maximum exposure limit to EM fields generated by microwaves at an irradiance of 50 W/m2, recognising the potential risks for human health at higher levels. A review from various proposals reveals that the maximum irradiance frequently exceeds this limit, as summarized in Table 2. However, in some cases, precise irradiance values are not clearly reported [14].

The biological and behavioural effects of high microwave irradiance in animals have been reported in the literature [66], [67]. The most significant short-term effect is the increase in the temperature of exposed animals. For instance, a study on rabbits found that they experienced an average temperature increase of 1,5 ºC after two hours of continuous exposure to 250 W/m2. These rabbits exhibited symptoms of thermal distress, while those exposed to 100 W/m2 for four hours did not show any relevant symptoms [68]. Similar

thermal distress has been observed in birds after 200 minutes of exposure at 250 W/m2 and after 20 minutes of exposure at 1000 W/m2, although no significant behavioural changes were noted [69].

Table 2. Maximum irradiance for different SBSP proposals.
Maximum irradiance allowed by the EU indicated in grey.

SBSP Proposal	Country	Irradiance $[\frac{W}{m^2}]$	[Ref.]
Solar Umbrella	U.S	0.023	[60]
MR-SPS Demonstrator	China	20	[70]
EU exposure limit	EU	50	[65]
CASSIOPeiA	United Kingdom	230	[71]
NASA 1974	U.S	300	[57]
MR-SPS	China	460	[72]
Tethered-SPS	Japan	1,000	[73]

2.3.2 Development by country

The strategic importance of energy sources, particularly those that are free of CO_2 and pollution during operation, has led to a sustained interest in SBSP. This global interest has resulted in several countries to take independent or international collaborative initiatives. This section presents an overview of the current progress of SBSP development by different nations and international organisations.

2.3.2.1 United States of America

The concept of SBSP was first introduced by Peter Glaser in 1968 [55], and this idea gained attention from NASA, which published a first report in 1974 asserting the technical and economic feasibility of SBSP [57]. The report identified several critical technologies required for the project to become viable both in terms of performance and cost. These included the necessity for efficient solar energy conversion systems capable of functioning

at elevated temperatures, methods for long-range microwave power transmission, and techniques for the assembly and control of large, semiflexible spacecraft structures.

In the aftermath of the 1973 oil crisis, the U.S. government identified the urgent need to develop new methods for generating large amounts of electricity. This led to the identification of the SBSP concept as a promising approach to explore. Consequently, in 1977, NASA and the U.S. Department of Energy launched a joint programme to further define and investigate the feasibility of SBSP. The objective of this initiative was to provide a comprehensive evaluation of the technology and enable policymakers to decide whether to advance its development [74]. By 1980, the results of this joint programme were presented and published, covering a wide range of topics including system definition, structure design, assembly processes, transportation to orbit, sizing, method of power conversion and transmission, environmental implications, public concern and economic costs, among others [75].

In view of the substantial economic expense, the U.S. government made the decision to discontinue major development projects and conduct a re-evaluation the proposal a decade later. In 1995, SBSP was reconsidered, with a focus on evaluating technological advancements and novel system architectures to determine their economic feasibility. Advances in microwave generation, photovoltaic cells and reduced transportation costs contributed to the initiation of a new concept definition study [76]. Over the following years, research initiatives were directed towards the maturation of the critical technologies, with a particular emphasis on the development of microwave power transmission systems [77].

In 2019, the Air Force Research Laboratory initiated the Space Solar Power Incremental Demonstrations and Research project (SSPIDR) with the objective of exploring and developing key technologies for SBSP [78], [79]. The aims to investigate and advance capabilities that could enable reliable and sustainable energy transmission from space for use by military forces. The main experiment within SSPIDR is the development of an experimental SBSP named Arachne, which is scheduled for launch in 2025. Due to the military nature and ongoing development status of the project, specific details remain undisclosed.

Until today, the most recent report on SBSP, published in 2024, addressed two fundamental questions: the conditions under which SBSP could become a competitive

option for achieving net-zero greenhouse gas emissions compared to other renewable energies sources, and the potential role NASA might play in its development [2]. The report highlighted a key challenge: the substantial effort required to develop the technologies necessary to autonomously operate, assemble and manufacture a massive SBSP system in orbit, a scale never before achieved in space. While the implementation of SBSP using current or near-term technologies incurs substantial costs, the study determined that SBSP has the potential to generate greenhouse gas emissions that are comparable to those of existing renewable energy sources, such as hydropower or photovoltaic plants with lithium battery storage [2].

Additionally, the report proposed two strategic options for NASA. The first option is to continue investing in technology development to enhance the feasibility of SBSP over the long term. The second option is a more proactive approach for NASA, involving the formation of partnerships with other national agencies, space agencies from other countries such as ESA or JAXA, or collaboration with private sector entities to advance the development of SBSP systems.

2.3.2.2 Europe

Following the initial report by NASA on the feasibility of SBSP in 1974, the concept attracted significant interest from various European research centres, particularly in West Germany, the United Kingdom and France. The primary focus of these studies was on evaluating the potential benefits of SBSP, its integration into the energy grid, and a comparison with the U.S. with respect to the location of ground stations. However, several concerns were raised, particularly regarding the environmental impact and the geographical constraints of locating the ground stations. The higher population density and higher latitudes of major population centres in Europe would require higher exclusion areas due to higher irradiance levels in comparison to the U.S. [80]. One proposed solution to avoid populated areas was to locate the rectennas on offshore platforms [81].

In 1978, ESA initiated its interest in SBSP [82], and by 1979, it had conducted the first preliminary study on the concept [83]. The study provided a comprehensive review of the SBSP concept and system architecture, examining the state of the art of the technologies available at the time, identifying specific requirements and indicating the improvements

necessary for implementation, including HV-DC power conditioning and distribution. The study also addressed several non-technical concerns, such as safety, environmental effects, potential interference with telecommunication systems, and the regulatory and political challenges associated with orbital allocation. Ultimately, the study concluded that while SBSP had the potential to be economically viable, its development and deployment would require a close partnership with the U.S. Without such collaboration, the realization of a full-scale SBSP system would be unlikely.

During the following decades ESA deprioritised the development of SBSP. However, in 2003, the agency revisited the concept and initiated a new programme with the goal of evaluating its viability, identifying potential system candidates, and exploring its potential applications for space exploration [84]. As part of this initiative, an economic viability study of SBSP was conducted in 2005 [85]. The study concluded that SBSP could be competitive with terrestrial renewable energy systems, such as photovoltaic systems paired with hydrogen storage, but only with the deployment of a large platform with a capacity of 100 to 150 GW. It was estimated that the energy required to develop, manufacture, and deploy an SBSP platform could be compensated in one year of operation, given the energy it would generate. The study highlighted that the predominant factor influencing the competitiveness of SBSP in comparison to terrestrial renewable solutions was the cost and frequency of launch to orbit.

During this period, various technologies for the deployment of large structures in space were explored [86], including a demonstrator to test the feasibility of deploying large, flexible net structures in orbit [87]. SBSP has also been proposed as a potential solution to address the challenges of lunar nights, which can last 15 days. This period of darkness complicates the energy generation for scientific missions or potential human settlements, and in this context, SBSP is considered as a viable alternative to nuclear energy [88].

Following a period of research and key technologies testing during the early 2000s, ESA launched the SOLARIS initiative at the end of 2022 [89]. The initiative focuses on conducting systems studies, advancing technology development, and undertaking research activities to mature the essential technologies required for SBSP, thereby contributing to the achievement of net-zero greenhouse gas emissions by 2050. The results and data gathered from the SOLARIS programme are expected to provide a solid basis for a decision by 2025 on whether to proceed with preparations for a potential SBSP demonstrator mission.

As the foundation of the SOLARIS initiative, two viability studies were conducted in 2022 to assess the economic and technological feasibility. The first study, conducted by Frazer-Nash consultancy [90], used the CASSIOPeiA concept sized at 1,44 GW SBSP as a reference [71]. The study evaluated the state of the technology and determined that substantial advancements in solar collection, microwave power transmission, and in-orbit assembly would be required to reach operational readiness by 2040. For a full-scale prototype, the production and implementation were estimated at four years, with an approximate cost of €6,8 billion.

The second feasibility study, carried out by the company Roland Berger [91], utilised the SPS-Alpha MK III SBSP concept, sized at 2 GW, as its point of reference [92]. The study identified various technological challenges, including the development of all elements necessary for converting sunlight to microwaves, the assembly and maintenance of large-scale structures in orbit, and the implementation of robust space debris mitigation systems. The total estimated cost, considering the launch, the SBSP platform, and the ground systems, was reported to range between €8,1 and €33,4 billion.

The findings of both studies indicated that SBSP has the potential to contribute towards the achievement of net-zero greenhouse gas emissions, while complementing renewable energy sources such as photovoltaic farms and wind turbines. However, the studies highlighted concerns regarding the significant technological improvements required to meet the specifications of a full-scale implementation, as well as the substantial costs involved, particularly regarding launch vehicles.

As part of the SOLARIS programme, two SBSP platform concepts have been proposed. The first, developed by Thales Alenia Space [14], involves a 1 GW SBSP platform located in GEO, utilising microwave wireless transmission. The EPS design includes a SAS operating at 400 V – 500 V, employing perovskite solar cells with a total surface area of 6,2 km^2. The generation of power from the SAS is regulated by a S3R, and the voltage is elevated to 20 kV for the distribution bus. The estimated cost of this SBSP is $11,4 billon. Furthermore, a scale-down demonstrator has been proposed, ranging from 72 kW to 200 kW of power generation in orbit.

The second concept, developed by the company Arthur Little, proposes an alternative approach for SBSP involving a constellation of 3.987 reflectors in Sun Synchronous Orbit

(SSO). Instead of the use of solar arrays, this approach focuses on reflecting sunlight to photovoltaic power plants on Earth's [63]. It is estimated that the power generation could reach 0,4 GW for a small ground station and up to 5,6 GW for a large ground station. Each reflector is designed as a 1 km diameter disk with a reflective surface. The power requirements for this system are considerably lower in comparison to photovoltaic-based SBSP platforms, estimated at around 280 W per reflector. The power consumption is primarily attributed to the attitude control and the onboard computer. The total estimated cost for the entire system, including design, production, launch and assembly, is approximately €54,4 billion.

2.3.2.3 Japan

The Institute of Space and Astronautical Science (ISAS) – the organization that would later merge with JAXA – initiated the exploration of SBSP platforms in the 1980s as a potential solution to combat climate change. This interest culminated in the development of their first SBSP proposal in 1993, known as SPS 2000 [93]. In contrast to the SBSP concepts proposed by the U.S. and Europe during the same period, SPS 2000 was conceptualised as a scaled-down LEO SBSP platform with 10 MW power generation, and the electrical design included 1 kV SAS and distribution bus.

However, interactions with space plasma at these voltage levels resulted in material degradation in the insulator and structural components. To address these challenges, laboratory studies were conducted to investigate the degradation mechanisms at various altitudes [93]. The findings from this study aimed to provide guidelines for the design and sizing of the insulators and harness for the SPS 2000. The development of the SPS 2000 progressed further, leading into the construction of two scaled-down electrical functional models capable of power generation and microwave wireless transmission in laboratory conditions [94].

In 2005, JAXA unveiled a pioneering proposal for a 1,2 GW SBSP concept known as Tethered-SPS [73]. The innovative design featured a 3,8 km^2 platform suspended by a multi-wire tether extending 10 km from the bus. The platform consists of 9.500 interconnected modules, each one capable of transmitting microwaves at 420 W. Each module is integrated with solar cells on both sides, a PCU, batteries, and the microwave transmission system.

Synchronisation and communication among the modules are achieved through a wireless LAN system.

In subsequent years, JAXA undertook the development of various demonstrators to advance in microwave wireless power transmission technologies within the kW power range and beam-pointing accuracy [95]. By the end of 2024, a long-range wireless power transfer demonstration had been successfully carried out [96]. This experiment involved mounting a microwave antenna on an aircraft fairing. The altitude was 7 km, and the speed 700 km/h. A beam of 270 W was directed towards an open field equipped with 13 rectennas spaced 600 meters between. The results confirmed the feasibility of transmitting wireless power over long distances with precise control of the transmitting beam.

In 2025, two technology demonstrators are planned to be launched, with a focus on key technologies for the Tethered-SPS platform. The first mission, designated as DELIGHT, aims to test the deployment mechanism of an 8 m^2 folded antenna, which could be used for constructing large space structures [97], [98]. The second demonstrator, designated as OHISAMA, is a small satellite in LEO capable of transmitting microwaves at hundreds of watts, with a potential application for future SBSP on the Moon [99]. The mission objectives include evaluating the architecture and performance of the SBSP system and testing the microwave beam control mechanisms. Additionally, it will demonstrate wireless power transmission between spacecrafts separated up to 50 meters. Finally, these experiments will allow to investigate the effects of high-power microwaves on the ionosphere.

2.3.2.4 China

From 1996 onwards, Chinese scientists began to consider the development of SBSP as a viable option for energy production [100]. This growing interest resulted in national support being initiated in 2008 when the China National Space Administration (CNSA) launched its research project, developing key technology for SBSP [101]. During this period, several studies were carried out to investigate high-power microwave transmission systems [102] and other key technologies, including JAXA's Tethered-SPS concept [103]. Based on these studies, two proposals were presented in 2014 as part of their strategic plan.

The initial concept, known as MR-SPS, was conceptualized by the China Aerospace Science and Technology Corporation (CASC). The MR-SPS proposes a 1 GW SBSP stationed in GEO with microwave power transmission [104]. The system incorporates multiple subarrays, each one equipped with 500 V SAS, subsequently converted to 5 kV. Finally, a HV converter increases the voltage up to 20kV and supplies the microwave transmission system [13].

The second concept, known as SSPS-OMEGA, was developed at Xidian University. Unlike the MR-SPS, the SSPS-OMEGA envisions a spherical structure composed of reflectors to concentrate sunlight onto the solar arrays [105]. The platform was 2 GW rated with microwave transmission and stationed in GEO. A functional ground demonstrator was created as part of the development process. This demonstrator was designed to validate the concept while integrating the reflectors, solar arrays, and microwave transmission system, achieving 2 kW of wireless power transfer [106].

In 2023, CASC introduced a modified version of the MR-SPS concept called MMR-SPS, which was developed to address the challenges associated with long-distance HV distribution buses, while maintaining the same 1 GW rating [72]. The original concept featured a centralized microwave and antenna system, whereas the new proposal, considers a modular distributed microwave system across the solar array modules. Each module in this configuration should handle 48 MW at most, simplifying power management and reducing harness from several kilometres to 300 metres. As a result, the distribution bus voltage is reduced to 5 kV, while the SAS remains at 500 V. However, the modular configuration requires precise control of the microwave beaming due to the geometry of the distributed antenna arrays. This added complexity necessitates advancements in beam forming and alignment technologies to ensure accurate power transmission.

The CNSA has outlined plans for a future in-orbit technological demonstrator mission to validate key technologies for the MR-SPS and SSPS-OMEGA concepts [107]. Scheduled for launch in 2026 [3], the mission will involve a main satellite generating and transmitting power, either to a second satellite or directly to a ground station. The EPS will be powered by two sources, a 500 V thin-film solar array and a solar concentrator designed to operate at 100 V, each one is expected to achieve 10 kW. Two types of power transmission will be tested, laser power transmission for intersatellite and ground station, and microwave power transmission for ground station.

2.4 DC/DC converters for high-voltage buses

Since the conceptualisation of the SBSP, research and development efforts have been made on advancing key technologies such as the deployment of large structures [108], high power DC to microwave conversion [109], and beam forming [61]. These efforts have contributed to the maturation of the SBSP concept. With regard to the EPS, the main subject of this thesis, various concepts suggest the use of 500 V SAS combined with distribution buses operating between 5 kV and 20 kV for GW power-range [13], [14]. Despite the proposals previously analysed in section 2.3.2, technical challenges associated with HV and high power conditioning and distribution for space environment remains underexplored.

First of all, conditioning from the SAS requires the selection of suitable DC/DC converter. In this sense, different requirements have been identified:

- **Current fed and output current source:** Current mode converters are simple to parallelize and connect to the voltage distribution bus. Solar arrays behave as current sources and long harness connection reinforce this behaviour, i. e. non-negligible harness inductance.

- **Galvanic isolation**: In large power structures, galvanic isolation is essential to isolate different zones, as well as to provide voltage level transformation.

- **Voltage regulation:** The converter must provide stable output voltage regardless of variations in the power generation or fluctuations on the load. In addition, it should be reliable in case of parameter variations.

- **Simple and reliable switching driving control:** It is convenient to simplify transistor driver and failure modes, thus, the selection of the topology is critical.

- **Modularity:** Due to the large number of SAS, a modular topology should be selected for an easier scalable solution and redundant implementation.

2.4.1 DC/DC converter structures review

The selection of the DC/DC converter is restricted to common structures. Four initial assumptions have been made; first, solar array section voltage is 100 V, which is the most common voltage in large platforms [5], [35], [38]. Despite several SBPS proposals envisaging the use of higher solar array voltage [13], [14], these are still under development and have serious reliability implications derived from HV issues [10], [11], [12]. The second assumption is that the output voltage is set at 300 V, aligned with the expected distribution bus voltage up to 180 kW [6]. The third assumption is that galvanic isolation is required. Finally, it is assumed that power flow is unidirectional, and thus a passive AC/DC structure is sufficient. A general schematic of the required DC/DC converter is shown in Figure 15.

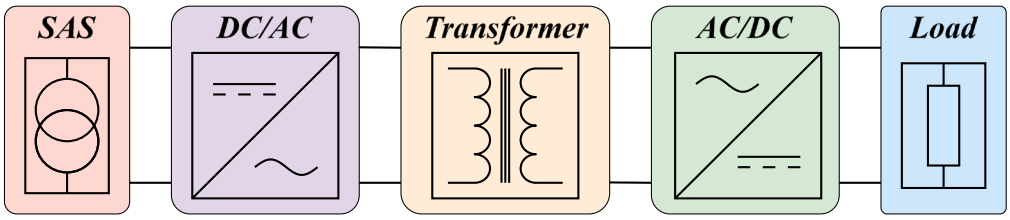

Figure 15. General DC/DC converter schematic.

Various power conversion structures are suitable for both DC/AC and AC/DC parts. As stated in ECSS-E-ST-20C [6], a failure of a single component must not propagate to other components or elements in the system, which leads to significant restrictions in the selection of topologies and their components. A comparison of the most common structures has been conducted in the following sections.

2.4.1.1 Inverter structure: DC/AC

Double-ended structures such as push-pull, half-bridge, and full-bridge are widely used in medium and large power isolated converters, as illustrated in Figure 16. For space applications, the selection of a particular structure is mainly driven by two factors, component availability and reliability. To select the structure, it is imperative to evaluate the maximum voltage and current values as well as the derating factors for the power semiconductors. In addition, an assessment of single-point failure should be conducted.

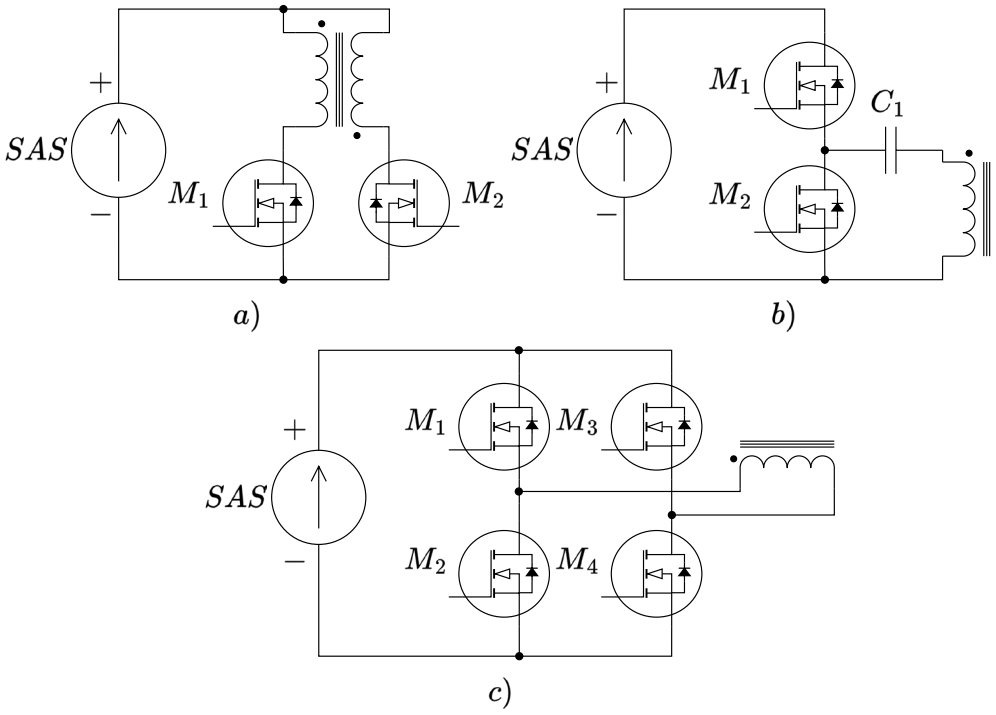

Figure 16. Double-ended inverter structures for isolated converters.
a) Push-pull, b) Half-bridge, c) Full-bridge

Table 3 summarizes the main characteristics of the inverter structure. In accordance with the ECSS-Q-ST-30-11C guidelines concerning FETs [33], a 80% voltage derating and a 75% current derating has been considered. As shown in Table 3, the push-pull structure requires an additional primary transformer winding, and its transistors must block twice the voltage of the other structures. However, it offers the advantage of having two low-side transistors, which simplifies the driver circuit. The half-bridge structure requires higher current rating and has half the transformer output gain compared to the other structures. However, it benefits from a low number of switches and a simpler transformer design. In contrast, the full-bridge structure requires more transistors in the low and high side. However, it maintains the lowest voltage and current ratings when compared to the push-pull and half-bridge structures.

Table 3. Electrical characteristics of the double-ended inverter structures

Parameters	Push-pull	Half-bridge	Full-bridge
No. switches	2	2	4
No. primary transformer windings	2	1	1
Required (after derating) V_{DSS}	$\frac{5}{2} \cdot V_{SAS}$	$\frac{5}{4} \cdot V_{SAS}$	$\frac{5}{4} \cdot V_{SAS}$
Required (after derating) I_D	$\frac{3}{4} \cdot I_{SAS}$	$\frac{3}{2} \cdot I_{SAS}$	$\frac{3}{4} \cdot I_{SAS}$
Transformer output gain (1:1)	1	1/2	1
Driving circuit	2·Low side	1·High side 1·Low side	2·High side 2·Low side

Three modes of failure are typically considered for power semiconductor switches: open, short-circuit and linear operation. This analysis has focused on the first two types. The limited open circuit voltage, V_{OC}, and short-circuit current, I_{SC} of the SAS facilitate the component sizing and contribute to the mitigation of failure propagation.

Due to the symmetry of the push-pull structure, the effects of a fault are identical whether it occurs in M_1 or M_2. If an open circuit fault occurs, then half of the power fails to transmit, resulting in a unipolar voltage square AC-wave applied to the magnetic core instead of a bipolar voltage square-AC wave. This situation rapidly leads to transformer saturation and a temperature increase. In the worst scenario, neighbouring components can be damaged. In the case of a short-circuit fault, power transfer is also interrupted, but the failure does not propagate since the SAS is a current-limited source. In this case, the SAS is shunted, and the primary windings of the transformer and the power semiconductor must withstand the maximum current, I_{SC}, which is also required in nominal operation.

The fault analysis in a half-bridge structure varies depending on whether the fault occurs in the high-side at M_1 or the low-side at M_2. When an open circuit fault occurs in the high-side switch, the SAS goes to V_{OC}, and power is not transmitted to the transformer. Conversely, if the open circuit fault is in the low-side transistor and the high-side transistor

is operating correctly, then the DC blocking capacitor, C_1, will charge until it reaches V_{OC}, ending up the power transfer. If a short-circuit fault occurs at the high-side transistor, then an uncontrolled resonant circuit will be generated between C_1 and L_m of the transformer. This oscillation will be transferred to the transformer's secondary side, potentially leading to system failure propagation. If there is a short-circuit fault at the low-side transistor, then the SAS alternates between open circuit and short-circuit, resulting in null power transfer.

In the full-bridge configuration, the power switches can be regarded as symmetrical concerning the fault state due to the balanced driving sequence. When an open circuit fault occurs in one of the switches, the transformer primary voltage shifts from a bipolar AC signal to unipolar AC signal, causing saturation on the transformer. If a short-circuit fault occurs, then the SAS will be shunted during a portion of the switching period when the other transistor in the branch is turned on, yet a unipolar AC signal continues to be generated and transferred during certain intervals, causing the saturation of the transformer.

Therefore, based on the fault analysis, the half-bridge structure is high risk due to the potential oscillations triggered by a short-circuit fault. The main issues associated with the push-pull and full-bridge structures lie with the generation of a pulsed waveform and the potential overheating because of the transformer core saturation. These issues can be addressed by incorporating under-voltage and over-temperature protections to isolate the fault. Whilst both structures are feasible; however, the push-pull structure is preferable due to its lower component count, and simpler driver design. The main drawback of the push-pull structure is the voltage rating of switches, which is twice the input voltage, but it is still suitable for space-qualified components operating with 100 V solar arrays [110].

2.4.1.2 Rectifier structure: AC/DC

Two passive rectifier configurations, as shown in Figure 17, are considered for the rectification in unidirectional isolated converters: the centre tapped full-wave rectifier and the full bridge rectifier. As in the inverter structure, the required component rating and the effects derived from a fault should be evaluated for the final selection.

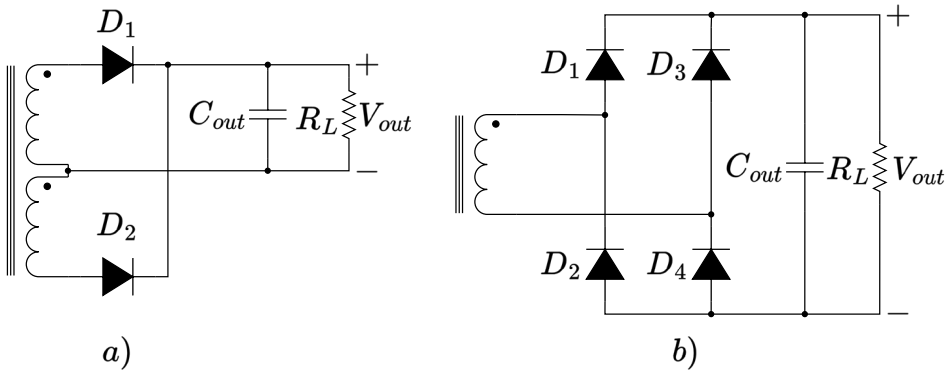

Figure 17. Passive rectifier structures for isolated converters.
a) Centre tapped full-wave rectifier, b) Full bridge rectifier.

Table 4 summarizes the main electrical characteristics of each rectifier structure. The analysis has considered a diode with a maximum V_{RRM} derated at 75% in compliance with the ECSS-Q-ST-30-11C guidelines [33]. Although the full bridge rectifier blocks V_{out} during rectification, to prevent failure propagation in case of short-circuit failure, the diode must be capable of handling double this voltage. Therefore, the diodes in both structures are required to block $\frac{8}{3} \cdot V_{out}$.

Table 4. Electrical characteristics of the secondary structures

Parameters	Centre Tapped full-wave	Full bridge
No. diodes	2	4
No. secondary windings	2	1
Required (after derating) V_{RRM}	$\frac{8}{3} \cdot V_{out}$	$\frac{8}{3} \cdot V_{out}$

Open circuit and short-circuit diode faults have been considered for the analysis. Regarding the centre tapped full-wave configuration, both rectifier diodes are symmetrical during operation, with their faults being identical. When an open circuit occurs, the power output is reduced by half, and the output ripple voltage increases. However, the rectifier remains operational under these conditions. Conversely, in the event of a short-circuit the bus capacitor would discharge through the secondary winding, causing an uncontrolled discharge of the output capacitor. To prevent this catastrophic failure, two series diodes must be used or a single diode connected at the output of the converter [111]. If an open circuit fault occurs in the full bridge rectifier, the power output is reduced by half, and the voltage

ripple increases. A similar power reduction and increase in ripple occurs in case of a short-circuit in one of the diodes but in this case the rectifier diode must be rated to withstand at least twice the output voltage to prevent the failure propagation.

It has been concluded that both options are viable for implementation. The centre tapped full-wave rectifier is preferable due to its reduced diode count. Nevertheless, this option has the disadvantage of requiring an increased number of windings in the transformer and the inclusion of an extra diode for protection.

2.4.2 Topology comparison

After the brief discussion on the double-ended basic structures, the selection of the complete topology and control method is required. The main requirements identified for the final selection are galvanic isolation, high-efficiency, possibility of parallelisation and serialisation, and a simple regulation. Thus, the following topologies have been considered: the Phase-Shift Full Bridge (PSFB), the Dual Active Bridge (DAB), the LLC resonant converter, and the ZVZCS-DCX converter.

2.4.2.1 Phase-shift full bridge

The PSFB converter, depicted schematically in Figure 18, is an isolated Zero Voltage Switching (ZVS) converter, wherein voltage regulation is accomplished by modulating the phase-shift between the control signals of one leg (M_1, M_2) and the other (M_3, M_4). This regulation method implies the use of a full-bridge structure on the primary side. Furthermore, as this is a voltage-fed converter, a capacitor, C_{in}, is required, which complicates the shunt operation of the solar array section if required.

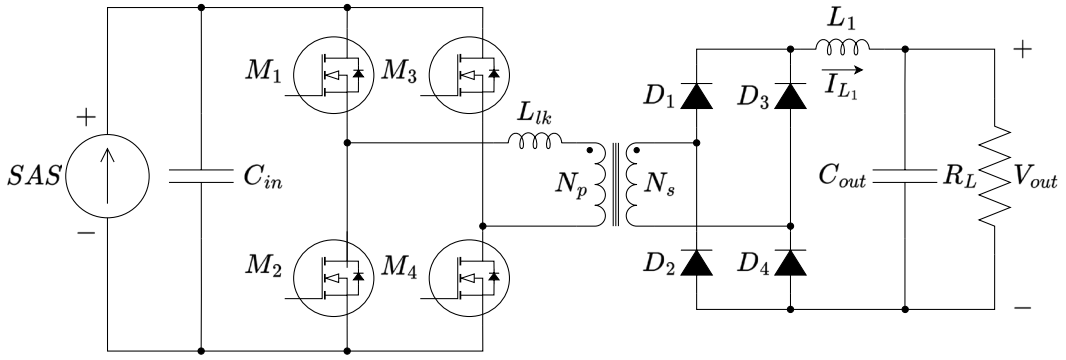

Figure 18. Schematic of the Phase-Shift Full Bridge topology.

Ideally, the PSFB transfer voltage gain, A_V, would be determined by the turn ratio of the transformer on the primary side, N_p, and secondary side, N_s, along with the duty cycle, D, of the phase-shift control signals. However, in practice, the duty cycle on the secondary side deviates from the primary side due to the leakage inductance, L_{lk}. As a result, A_V becomes dependent on additional factors such as the switching frequency, f_{sw}, the SAS voltage, V_{SAS}, the output inductance, L_1, and its current, I_{L1}, as well as the output voltage, V_o. As demonstrated in [112], the DC transfer function is given by (1). The multiple dependencies of A_V on these variables make it sensitive to variations caused by changes in irradiance or temperature affecting the SAS, as well as long-term drifts in L_1 or f_{sw} due to degradation.

$$A_V = \frac{N_s}{N_p}\left(D - \frac{N_s}{N_p}\cdot\frac{2L_{lk}f_{sw}}{V_{SAS}}\left(2I_{L1} - \frac{V_{out}}{2L_1 f_{sw}}(1-D)\right)\right) \quad (1)$$

As discussed in [113], the average model of the PSFB topology can be represented as a dependent current source at the input and the output ports. The output behaviour of the converter as a current source facilitates the parallelisation of multiple converters; however, output serialisation of converters would force synchronisation among each converter, which would significantly increase the complexity of the control [114].

2.4.2.2 Dual active bridge

The DAB is an isolated ZVS converter whose operation is derived from the PSFB. Here, the phase-shift is performed between the voltages of the primary and secondary sides. The

DAB requires an active full-bridge rectifier, as illustrated in Figure 19, although a passive implementation is feasible through a single active bridge topology [115]. Analogous to PSFB, the DAB functions as a voltage-fed converter, thus requiring a capacitor at the input, C_{in}.

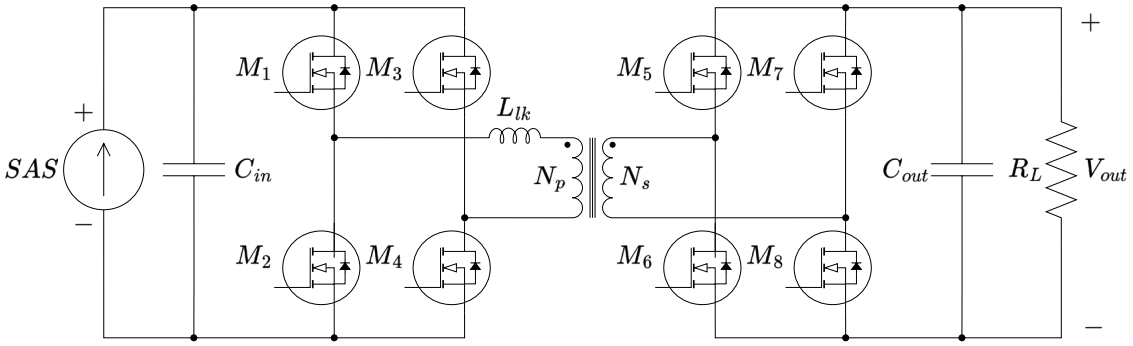

Figure 19. Schematic of the Dual Active Bridge topology.

The DAB has a simpler DC transfer function than PSFB, depending as expressed in (2) and discussed in [116]. However, it is still susceptible to variations of different circuit parameters.

$$A_V = \frac{N_s}{N_p} \cdot \frac{R_L}{2 f_{sw} L_{lk}} D(1 - D) \tag{2}$$

As discussed in [117], the average model of the DAB topology can be represented as a dependent current source at both the input and the output facilitating parallel connection of multiple converters. However, series output connection requires complex control algorithms for voltage equalisation [118].

2.4.2.3 Resonant LLC

The resonant LLC converter, represented in Figure 20 as a full-bridge structure, is an isolated Zero Voltage Zero Current Switching (ZVZCS) converter, where the voltage is regulated by varying the switching frequency relative to the resonant frequency of the network formed by C_r, L_r and L_m. Half-bridge and full-bridge structures are commonly found in LLC converters [119], [120], [121]. In addition, LLC converters have a proven track record in industrial applications, including photovoltaic systems [122].

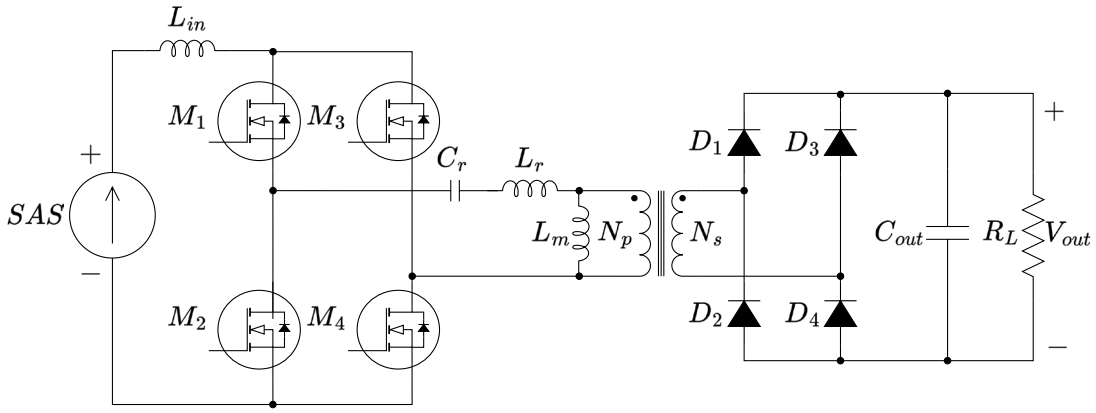

Figure 20. Schematic of the LLC topology based on the full-bridge structure.

The DC gain in the LLC converter (3) can be divided into the transformer turns ratio and the converter gain, G. The second part, G, is a complex function that depends on circuit parameters f_{sw}, R_L, C_r, L_r and L_m,. While A_V is sensitive to load variations, it can also be significantly affected by changes in C_r and L_r, which may degrade over time, leading to deviations in the voltage gain.

$$A_V = \frac{N_s}{N_p} \cdot G(f_{sw}, R_L, C_r, L_r, L_m) \tag{3}$$

The average model of a current-fed LLC topology can be represented as a dependent voltage source at the input and a dependent current source at the output, as discussed in [123]. However, output serialisation of converters would require balanced output voltages and resonant currents to ensure a reliable and efficient conversion when the outputs are connected in series. One method of ensuring voltage balance is to share the magnetic core, thereby linking the resonant circuit between the modules [124].

2.4.2.4 S3DCX

The ZVZCS converter presented in [125] can be viewed as a true DC transformer (ZVZCS-DCX), where the DC gain is the transformer turns ratio. It operates in open-loop and accommodates any type of double-ended structure [126], [127], [128], [129]. A push-pull implementation of the ZVZCS-DCX is depicted in Figure 21. This topology is a current-fed converter, which is beneficial for photovoltaic sources with long harness, as is the case in large satellites.

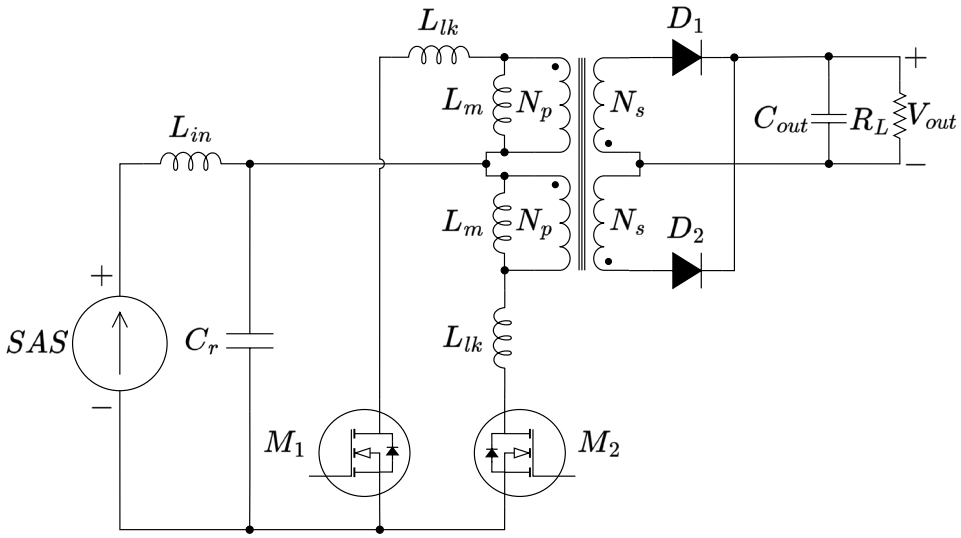

Figure 21. Schematic of the ZVZCS-DCX topology based on the push-pull structure.

While degradation or failure of resonant components and switching frequency can reduce the converter efficiency, these variations do not affect the transfer voltage gain, as expressed in (4).

$$A_V = \frac{N_s}{N_p} \tag{4}$$

The average model of the ZVZCS-DCX can be represented as a dependent voltage source at the input and a dependent current source at the output, as detailed in [125]. This current source behaviour at the output simplifies the parallel connection without additional control. For series connection at the output, the constant voltage gain simplifies the voltage distribution between modules, which can be maintained through synchronisation of different modules [130].

The ZVZCS-DCX is an unregulated converter, however, it is possible to establish regulation using several ZVZCS-DCX together with the S3R technique [9]. This concept, named –in this thesis for first time– as Sequential Switching Shunt DCX Regulator (S3DCX), is the consequence of two deeply rooted space-ideas. The S3DCX concept will be extensively described in the body of this doctoral thesis. To summarize the concept, an additional shunt transistor is included in parallel to the SAS, as depicted in Figure 22. The S3DCX provides regulation with the shunt transistor duty cycle, as the S3R. To ensure proper operation, the frequency of the shunt transistor must be significantly lower than the ZVZCS-DCX

switching frequency. Finally, the sequential operation of the S3R enables a scalable parallel connection of the converters.

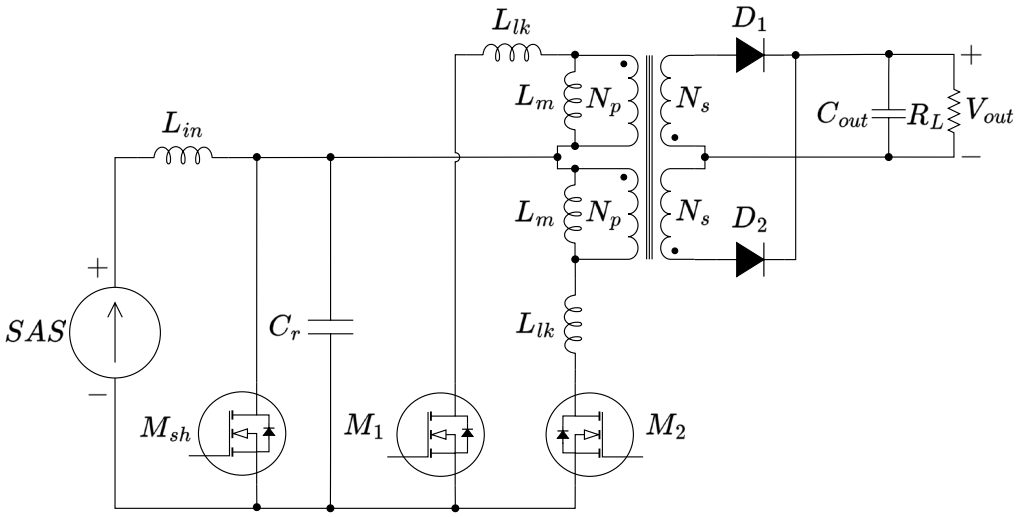

Figure 22. Schematic of the S3DCX using a push-pull structure.

2.4.3 Topology selection

Following the analysis in Section 2.4.2, a comparison of suitable topologies has been made, and the results are summarized in Table 5.

Table 5. Topology comparison regarding the requirements for the DC/DC converter. Legend: poor (−), normal (*0*), good (+).

Requirements	PSFB	DAB	LLC	S3DCX
Input current, output current	*0*	*0*	+	+
Voltage regulation	+	+	+	*0*
Robust transfer function	−	*0*	−	+
Simple driving control	−	−	*0*	+
Modularity	*0*	*0*	*0*	+

The main disadvantage associated to phase-shift control, such as PSFB or DAB, is the complex DC transfer function and sensitivity to circuit parameters. Additionally, the full-bridge implementation requires a complex control loop and drivers. LLC and S3DCX offer

greater flexibility in the primary-side structure and the push-pull structure is preferred due to its simpler driving circuit. Regarding the resonant tank, the capacitor is the most susceptible device to drift, but this can be mitigated by arranging in a matrix configuration [131]. Although the LLC topology has good performance and characteristics for its use, the S3DCX exhibits a much simpler and robust DC transfer function, which significantly simplifies the control loop. In conclusion, to close this chapter, the S3DCX is the preferred option for further study and implementation due to the aforementioned benefits.

Chapter 3

Article I: Sequential switching shunt regulation using DC transformers for solar array power processing in high voltage satellites

This chapter presents the first article that is part of the doctoral thesis, together with a comprehensive analysis of the results obtained.

Article I - [132], [133]**: Sequential Switching Shunt Regulation Using DC Transformers for Solar Array Power Processing in High Voltage Satellites.** ***IEEE Transactions on Aerospace and Electronic Systems*****, 60(1), 421-429,** Carlos Orts, Ausiàs Garrigós, David Marroquí and Andreas Franke

3.1 Summary

The following article presents a technique for solar array regulation for HV satellite power bus. The architecture is primarily intended for solar satellites, as discussed in Chapter 2, but it could also be applied to other high-power applications such as large telecommunication satellites or specific HV uses, like direct drive electric propulsion systems. The HV regulation is achieved by combining two well-known techniques in the European space sector: the ZVZCS converter [125], also called DCX because of its inherent DC transformer characteristics and the S3R [9]. Together, these form a power processing system named the S3DCX. The DCX converter provides a constant gain and galvanic isolation between the SAS and the distribution bus in an unregulated way. In order to achieve regulation at the output, different SAS are shunted sequentially based on a power balance. A power cell is defined as a single DCX combined with a shunt regulator that conditions a SAS. These power cells can have their outputs connected in series or parallel to achieve higher voltage gain or higher output current. Five power cells with N=3 voltage gain have been implemented. The voltage of each SAS is limited to 120 V and the nominal current is 4 A. The bus capacitance and the control loop are designed to satisfy the limit mask impedance defined in ECSS-E-ST-20C [6]. The article is divided into five sections, distributed as follows:

- The needs and requirements for high power satellites and a brief discussion of different types of converters are introduced in the **first section**.
- The working principle, along with an analytical analysis and the averaged linear model are described in the **second section**.
- The design of a 2 kW prototype and the simulations are detailed in the **third section**.
- The experimental results are reported in the **fourth section**.
- The conclusions of the work are discussed in the **fifth section** and the calculations are detailed in the **annex**.

3.2 Article

Sequential Switching Shunt Regulation Using DC Transformers for Solar Array Power Processing in High Voltage Satellites

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This article proposes a solar array regulation technique for a high-voltage satellite power bus. The regulation method combines ON–OFF control at low frequency, i.e., kHz range, of highly efficient isolated and unregulated dc–dc converters operating at high frequency, i.e., hundreds of kHz. Although this technique can adopt different implementations, this article deals with a hysteretic voltage control loop at low frequency, also known sequential switching shunt regulator (S3R), and unregulated, isolated, current-fed, zero-voltage, and zero-current push–pull dc–dc converters. Design guidelines and experimental validation are provided.

Manuscript received 3 July 2023; revised 19 September 2023; accepted 9 October 2023. Date of publication 17 October 2023; date of current version 9 February 2024.

DOI. No. 10.1109/TAES.2023.3325314

Refereeing of this contribution was handled by R. Meyer.

This work was supported by the European Space Agency under Grant 4000136441/21/NL/GLC/my.

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NOMENCLATURE

Acronyms

BCR	Battery charge regulator.
BCDR	Battery charge discharge regulator.
BDR	Battery discharge regulator.
DC	Direct current.
DC–DC	Direct current to direct current.
DCX	Direct current transformer.
DET	Direct energy transfer.
ECSS	European Cooperation for Space Standardization.
EMI	Electromagnetic interference.
EP	Electrical propulsion.
EPC	Electronic power conditioner.
GEO	Geostationary orbit.
HV	High voltage.
LEO	Low Earth orbit.
LV	Low voltage.
MEA	Main error amplifier.
MPP	Maximum power point.
MPPT	Maximum power point tracking.
PCU	Power conditioning unit.
PPU	Power processing unit.
SAS	Solar array section.
S3DCX	Sequential switching shunt DCX regulator.
S3R	Sequential switching shunt regulator.
SSR	Switching shunt regulator.
TWTA	Travelling wave tube amplifier.
ZCS	Zero current switching.
ZVZC	Zero voltage zero current.
ZVS	Zero voltage switching.

I. INTRODUCTION

Solar array regulation is a critical power conversion function for any spacecraft. Two main methods are dominant nowadays: MPPT dc–dc converters and SSRs. While the first approach is typical in low- and medium-power LEO and interplanetary missions using unregulated bus architectures, the second method is widely used in medium and high-power satellites for GEO satellites using fully regulated bus architectures, being the S3R [1], [2], [3], [4], the most common SSR employed. The fully regulated bus is realized by the PCU, which integrates the SSR, the BCR, and the BDR, as represented in Fig. 1(a) [5], [6]. In the European Space standard [7], 100–120 V dc bus voltage is recommended for power levels higher than 8 kW, hence, most of the space companies have adapted their products to this voltage for the largest platforms. However, 100 V starts to be inadequate for the actual needs, since the most powerful platforms already reach 20–25 kW, also motivated by the use of high-power EP systems [8]. Large bus current lead to high mass harness and considerable dc losses, but also impacts on the maximum bus impedance (Z_{bus}) and bus capacitor (C_{bus}) [7]. Furthermore, EP systems require high-power, high-voltage supplies, which are provided by the PPUs directly connected to the regulated bus. Two-level

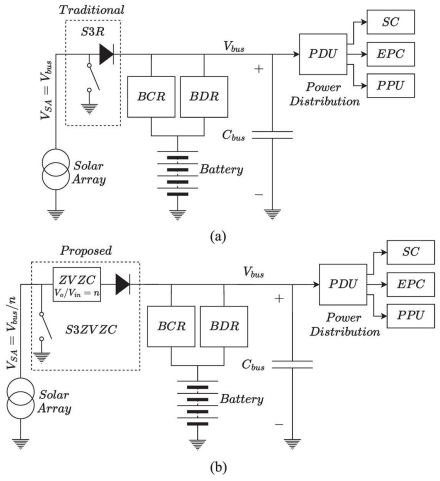

Fig. 1. High-power spacecraft electrical architecture. (a) Traditional [5]. (b) Proposed approach.

power conversion results in a penalty on efficiency and with obvious consequences on the thermal design, size, and mass. Besides, other systems, such as EPCs for TWTAs, also demand high-voltage supplies and could benefit of high voltage bus.

As a result, a higher bus voltage, around 300 V, is being considered, and two main approaches have been pondered to address its implementation. In [9], the solar array voltage is increased up to 300–350 V, and a DET connection from the solar generator to the electric thruster is suggested. The BCDR controls the bus voltage. While it is a conceptually simple solution, there are relevant technical challenges associated with the high-voltage solar array, such as arcing due to differential charging of the different materials, high-voltage slip rings, qualification, and cost [9]. Furthermore, it is a costly solution that requires full requalification of the solar array if the bus voltage is changed. In [10], a two-stage approach is proposed for an ion-thruster supply with MPPT tracking. The main advantages of this approach are the simplicity and heritage, since only well-known power regulators are used for its implementation. Besides, it exhibits very good regulation for large power transients that happen in ion-thrusters. The main disadvantage is the efficiency penalty due to S3R diodes and the Weinberg converter losses.

In [11], a two-bus approach is presented, implementing a high-voltage bus (HV_{bus}) at 450 V, and low-voltage bus (LV_{bus}) at 100 V, featuring an integrated power processing dc–dc converter. The power cell can operate in different operating modes, including MPPT and bus regulated for both busses, HV_{bus} and LV_{bus}. However, it requires a complex power processing dc–dc converter and control, making the practical implementation difficult with space-qualified electronic parts.

In this work, as presented in Fig. 1(b), a different approach for the solar array regulator is proposed. It uses highly efficient, isolated, unregulated, constant gain, high-frequency dc–dc converter, also known as "DC-Transformer" (DCX). The DCXs, switching at hundreds of kHz or more, are controlled as traditional S3R power cells at low frequency, i.e., kHz range, [1], [12]. This concept is adaptable to any regulated or unregulated bus. The design of BCRs and high-power BDRs [13], [14] are topics already discussed in the literature, therefore, these will not be covered in this work.

Different DCX topologies have been proposed for industrial, medical, telecommunications, and many other areas. Resonant techniques [15], and particularly the *LLC* converter [16], [17], have been widely accepted, but these are mostly oriented to have regulated outputs with complex control loops. Another type of unregulated DCX with ZVS and ZCS are described in [18] and [19]. Both converters use the magnetizing current of the transformer to achieve ZVS for all switches, but the method to achieve ZCS is slightly different. In [18], the leakage inductance of the transformer resonates with the output capacitor to achieve ZCS without any inductor. In [19], the converter is current-fed and the resonant circuit is formed by the leakage inductance and a resonant capacitor placed at the input. A fundamental feature of these DCXs is that the conversion gain is just the transformer turns ratio, so they are very simple and robust to parameter drifts. A detailed analysis of those types of DCX can be found in [20]. In the case at hand, the method proposed in [19] is better suited than the one described in [18], because a photovoltaic source inherently behaves as a current source below its MPP. This is also reinforced by the fact that the solar array harness inductance is relatively large in high-power satellites. Besides, a large capacitor is required as the main bus capacitor at the secondary side to fulfill the output impedance requirements [7]. As discussed in [20], any dual-ended topology is suitable, but current-fed ZVZC push–pull is widely used in satellite applications, mainly in EPC for TWTA [19].

In summary, the proposed S3DCX has the following benefits when compared to the existing solutions.

1) It is a simple concept that can be implemented with different DCX topologies, allowing voltage decoupling between solar array and distribution bus, which overcomes the limitations of the direct energy transfer regulators and provides increased flexibility in solar array design.
2) Higher (or lower) bus voltage could be achieved with very high efficiency (>95%) end to end.
3) It can be used as direct replacement of the S3R with minimum changes in regulated or unregulated bus architectures and variations.
4) It is highly modular and accepts parallel and series connection of isolated secondary sides to achieve higher current and voltage.

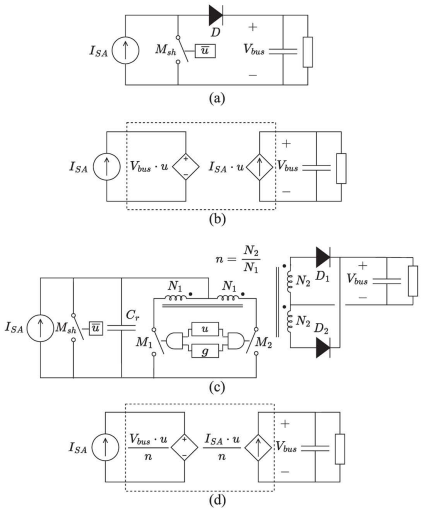

Fig. 2. DET shunt regulator. (a) Simplified schematic. (b) Large signal averaged model. DCX (current-fed ZVZC push–pull). (c) Power cell schematic. (d) Averaged model.

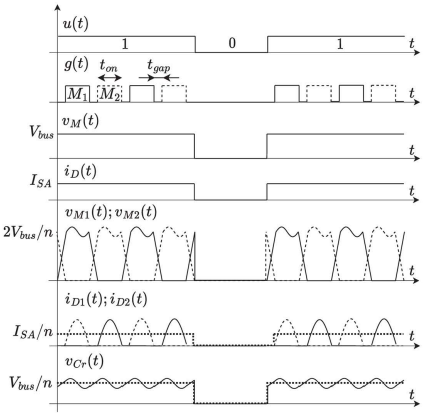

Fig. 3. DET and DCX main waveforms sketch.

The rest of this article is organized as follows. Section II introduces the S3DCX power cell as well as a particular implementation and modeling of the regulator. Section III details the design and simulation of the S3DCX for a 300 V–2 kW prototype. Section IV details the experimental validation of the proposed prototype and discusses the results. Finally, Section V concludes this article.

II. S3DCX: POWER CELL AND REGULATOR

The current-fed ZVZC push—pull, represented in Fig. 2(c), is considered as DCX for this work. Briefly, the main benefits of the selected topology are as follows.

1) Galvanic isolation provides easy adjustment of required output by transformer turns ratio and possibility of secondary side output connections (series and parallel).
2) It takes advantage of the natural solar array behavior and harness inductance to have a nearly constant current source.
3) It uses for its advantage all the parasitic elements of the transformer in a resonant manner, resulting in a very compact, simple, lightweight, and high efficiency solution.
4) All power semiconductors are operated in ZVS and ZCS.
5) ZVS and ZCS (neglecting magnetizing current) are load independent in a wide range.
6) Simple and low loss gate drive (rad-hard driver implementation is not linked to any complex driver integrated circuit).
7) Good power semiconductor utilization (>75% equivalent duty cycle).
8) Operation at fixed frequency and duty cycle (very simple and robust drive pulse generation).
9) Reduced number of components.
10) Very low EMI.

Fig. 2(a) and (b) represents the schematic and the large signal averaged model for the DET shunt regulator, respectively, and Fig. 2(c) and (d) shows the circuit schematic and averaged model of the proposed DCX. The control signal, u, dictates the power transfer from the solar array to the main bus in both cases (1), but the working principle is slightly different. When $u = 1$, in the DET case, the transistor $M_{\rm sh}$ is OFF and the diode D connects the solar array section to the bus, while in the DCX, the M_1 and M_2 driving pulses, g, operating at switching frequency, f_s, enable the power transfer. When $u = 0$, the transistor $M_{\rm sh}$ shunts the solar array in the DET and the DCX power cells. An important difference is that DCX allows voltage and current conversion ratio (gain is transformer turns ratio, n) when it transfers power to the bus, as it can be noted in the DCX averaged model. The main waveforms of the power cells are represented in Fig. 3, being from top to bottom: shunt driving signal, u; DCX driving signal, g; $M_{\rm sh}$ drain-source voltage of DET shunt regulator, v_M; diode current of DET shunt regulator, i_D; M_1 and M_2 drain–source voltage of DCX, v_{M1}, v_{M2}; rectifier diode current of DCX, i_{D1}, i_{D2}, and resonant capacitor voltage of DCX, v_{Cr}. M_1 and M_2 can be also used to perform power control transfer, u, and therefore one transistor is saved, however, $M_{\rm sh}$ simplifies

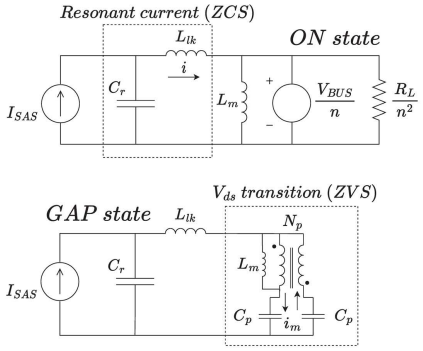

Fig. 4. DCX equivalent circuits for ON and GAP states.

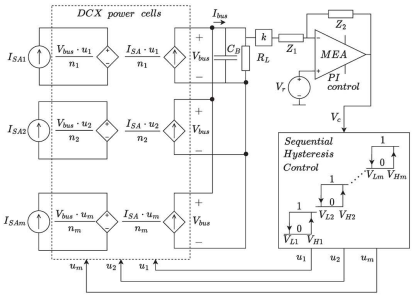

Fig. 5. S3DCX: Sequential hysteresis control scheme.

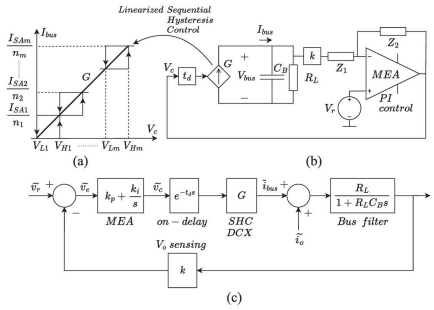

Fig. 6. S3DCX. (a) Linearized sequential hysteresis control. (b) Small-signal linear model. (c) Voltage feedback loop.

current limiting during shunt operation

$$u(t) = \begin{cases} 1: & SA \quad \text{power transfer} \\ 0: & SA \quad \text{shunted.} \end{cases} \tag{1}$$

The working principle of the DCX can be explained with the two equivalent circuits shown in Fig. 4. During the ON state, i.e., M_1 or M_2 is in conduction, a resonant switch current occurs due to the resonant circuit formed by the resonant capacitor, C_r, and the transformer leakage inductance, L_{lk}. During the GAP state, i.e., M_1 and M_2 are turned-OFF, the magnetizing current charges and discharges all the parasitic capacitances, i.e., MOSFETS, diodes, and transformer.

The analysis of the ON state circuit results in the resonant current, i, whose governing differential equation is given by (2). MOSFET current is $i_M = i - i_m$, being i_m, the magnetizing current and diode current is $i_D = i_M/n$

$$L_{lk}C_r\frac{\partial^2 i}{\partial t^2} + i = I_{SA}. \tag{2}$$

On the other hand, the analysis of the GAP state results in the governing differential (3), where the resonant circuit is formed by the magnetizing inductance, L_m, and the parasitic capacitance, C_p, given by (4). C_M is the parasitic MOSFET capacitance, C_{TR} is the parasitic transformer capacitance and C_D is the diode capacitance referred to the primary side

$$L_m C_p \frac{\partial^2 i_m}{\partial t^2} + \frac{i_m}{2} = 0 \tag{3}$$

$$C_p = C_M + C_{\text{TR}} + C_D \cdot n^2. \tag{4}$$

The detailed design procedure to solve (2) and (3) for ZVS and ZCS conditions can be found in the Appendix. It is clear from the ON state equivalent circuit that $<V_{Cr}> = V_{\text{bus}}/n$, implying that the solar array operating point, and therefore, the power injected to the bus, can be controlled by the bus voltage in closed-loop operation.

Satellite solar arrays are typically divided into several sections, i.e., an arrangement of several solar cell strings in parallel. In the proposed regulator, each section is attached to one DCX, refer to Fig. 2(c). In a sequential control scheme, some DCX converters are permanently ON providing power to the bus, while others DCX are OFF and only one DCX is turning ON and OFF to eventually perform output voltage regulation. This can be achieved by sequential hysteretic control [1], as illustrated in Fig. 5, being this scheme one of the most common methods employed in solar array regulation for medium and large satellites.

The linearized model of the S3DCX regulator is given by (5), resulting in a voltage-controlled current-source that supplies the main bus capacitor, represented in Fig. 6. The voltage loop gain, $T_v(s)$ and the closed-loop output impedance $Z_O(s)$ are given by (6) and (7), respectively

$$G = \frac{I_{\text{bus}}}{V_c} = \frac{\sum_{i=1}^{n} I_{SA_i}/n_i}{V_{Hm} - V_{L1}} \tag{5}$$

$$T_v(s) = kG\frac{k_p\left(s + k_i/k_p\right)}{s}\frac{1}{C_B\left(s + (1/R_L C_B)\right)} \tag{6}$$

$$Z_O(s) = \frac{\tilde{v}_o}{\tilde{i}_o} = \frac{1}{C_B\left(s + (1/R_L C_B)\right)[I + T_v(s)]}. \tag{7}$$

To avoid phase and gain margin degradation, [21], the regulator turn-ON delay, t_d, must be smaller than $1/\omega_c$, being

TABLE I
S3DCX: Main Design Parameters

Description	Value	Comment
Solar array section (SAS) – Agilent E4351B simulator		
V_{OC}	120V	Open-circuit voltage
V_{MP}	110V	Maximum power voltage
I_{SC}	4A	Short-circuit current
I_{MP}	3.9A	Maximum power current
P_{MP}	429W	Maximum power
C_{SAS}	200nF	Agilent E4351B
L_h	33µH	Added inductance
DCX transformer – push-pull (N_1=N_{1a}=N_{1b}; N_2=N_{2a}=N_{2b})		
Core	RM14	Material 3C95
n=N_2/N_1	15/5	V_{SAS}=100V; V_O=300V
DCX & shunt – circuit		
C_r	0.5 µF	CB182G0105J
M_1; M_2; M_{sh}	IXTQ42N25P	Si MOSFET (250V, 42A)
D_1; D_2	STPSC10H12	SiC diode (1.2kV, 10A)
t_{on}	2.8µs	f_s=135kHz; D=0.378
t_{gap}	0.9µs	f_{output}=270kHz
R_{cl}	50mΩ	Max shunt current= 14A
Control loop		
k	$4.08 \cdot 10^{-3}$	ADUM3190, V_{ref}=1.225V
k_p	298.8	Split into three stages
k_i	$97.96 \cdot 10^3$	
t_d	< 25µs	
G	1.11	
R_L	> 45Ω	P_{Omax}=2kW; V_O=300V
C_{BUS}	400µF	B32778G1206K000

ω_c the crossover frequency of the loop gain (6), $|T_v(j\omega_c)| = 1$. The closed-loop output impedance is constrained by the output impedance mask, defined in the standard [7], clause 5.7.2.o.

III. DESIGN, SIMULATION, AND PROTOTYPE IMPLEMENTATION

A 2 kW, five power-cell S3DCX regulator has been designed, simulated, and implemented. Detailed step-by-step calculations are included in the Appendix.

A. Design

The main characteristics of the S3DCX regulator and the solar array simulator are summarized in Table I.

Based on the simplified transformer circuit model shown in Fig. 7, measured parameters for the five transformers are included in Table II. These parameters are, magnetizing inductance L_m, leakage inductance L_{lk}, parasitic capacitance of the transformer C_{TR}, resistance of the primary R_1 and secondary winding R_2, and resonant frequency f_{res}.

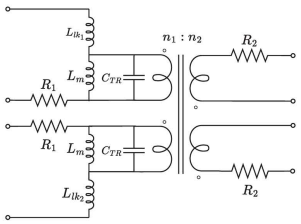

Fig. 7. S3DCX: Transformer equivalent circuit model.

TABLE II
S3DCX: Transformer Characterization

L_m [µH]	L_{lk1} [nH]	L_{lk2} [nH]	C_{TR} [pF]	R_1 [mΩ]	R_2 [mΩ]	f_{res} [kHz]
172.8	650	680	235	9.7	41.6	789
174.5	680	610	211	9.1	40.9	830
169.7	765	690	174	9.3	41.6	925
168.9	590	625	162	11.8	41.2	962
165.1	590	630	201	13.1	41.9	874

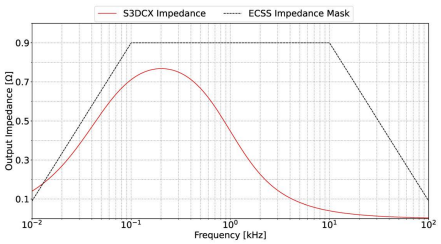

Fig. 8. S3DCX output impedance and ECSS impedance mask [7].

B. Simulation: Switching and Large-Signal Averaged Models

Computer simulation models have been implemented for both, switching and large-signal averaged versions. The output impedance of the S3DCX, which meets the impedance mask required by the European space standard [7], clause 5.7.2.o., is represented in Fig. 8.

A half bus power load step simulation is shown in Fig. 9. Nominal bus voltage ripple and bus voltage transient meet the European space standard [7], clauses 5.7.2.m and 5.7.2.i.1, respectively.

The S3DCX prototype is shown in Fig. 10. The five DCXs are identical, and the output connections are hard-wired to allow independent or series connections to the output bus capacitor, which is external and not shown in the figure. The MEA is implemented using an isolated error amplifier, and t_{on} and t_{gap} signals are obtained using only discrete electronic parts.

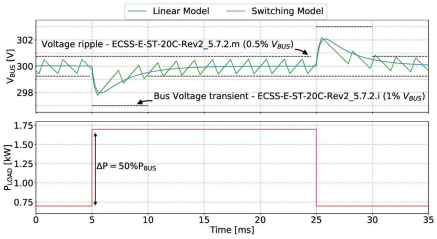

Fig. 9. S3DCX transient response simulation results. Top figure: Output voltage (switching and large-signal averaged models). Bottom figure: power load step.

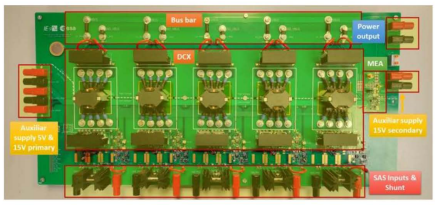

Fig. 10. S3DCX prototype: 2 kW, five power cells.

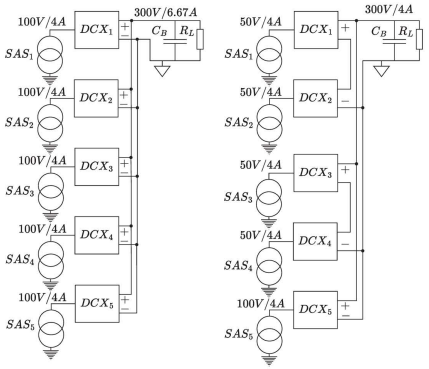

Fig. 11. Left figure: S3DCX five-independent output configuration. Right figure: Two solar array sections with two DCX in series and one independent.

IV. EXPERIMENTAL VALIDATION

Several tests have been carried out to validate the proposed solar regulation concept using independent and series configurations at the output of the regulator, as represented in Fig. 11.

A. DCX: Shunt and ZVZC Operation

Fig. 12 shows the detail of the ON (u = 1) and OFF (u = 0) of the DCX. It is clearly observed from the MOSFET voltage and diode current that ZVS and ZCS are achieved even during the transients. Besides, ON-delay, t_d, is limited to 18 μs. It can be also noticed that the shunt transistor goes into current limitation mode during the OFF action to discharge the parasitic capacitance of the solar array and the resonant capacitor of the DCX.

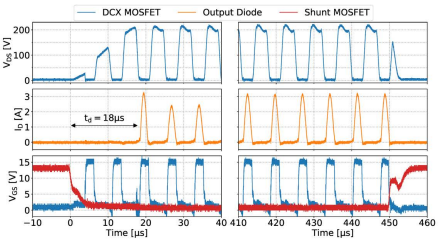

Fig. 12. Left: DCX ON detail. Right: DCX OFF detail. Top: V_{DS} M_1, Middle: I D_1, Bottom: Blue trace: V_{GS} M_1, and Red trace: V_{GS} shunt transistor.

TABLE III
DCX: Efficiency Measurements

I_{SAS} [A]	DCX1 [%]	DCX2 [%]	DCX3 [%]	DCX4 [%]	DCX5 [%]
1	92.5	92.5	92.0	91.9	92.0
2	95.3	95.2	94.8	94.8	94.8
3	95.9	95.3	95.5	95.4	95.5
4	95.8	95.8	95.4	95.1	95.3

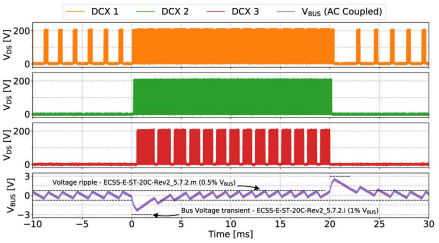

Fig. 13. S3DCX voltage regulation. Top: DCX 1: V_{DS} M_1; Middle-top: DCX 2: V_{DS} M_1; Middle-bottom: DCX 3: V_{DS} M_1; Bottom: bus voltage (ac coupled).

B. DCX: Efficiency

The efficiency of each DCX has been measured at different solar array currents, which could represent different irradiance levels or different solar array orientation, refer to Table III. Efficiency measurements also include power consumption of ancillary electronics and is close to 95.5% in nominal operation.

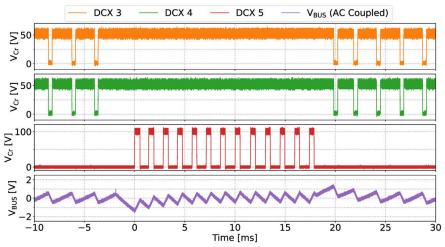

Fig. 14. S3DCX voltage regulation—output series connection. Top: DCX 3: V_{Cr}; Middle Top: DCX 4: V_{Cr}; Middle Bottom: DCX 5: V_{Cr}; Bottom: bus voltage (ac coupled).

C. S3DCX: Voltage Regulation

Fig. 13 illustrates the regulator's response under a 1 kW load power step, from 100 W to 1.1 kW (50% of the bus power). The configuration of the S3DCX is the one indicated in Fig. 11(left). At the beginning, DCX 1 is regulating the output voltage and the rest of DCX are fully OFF. Once the load step happens, DCX 1 and DCX 2 go to fully ON and DCX 3 regulates the output voltage. As it can be observed in the ac bus voltage waveform (bottom), the steady-state bus voltage ripple does not exceed the 0.5% of the nominal bus voltage (1.5 V) and the peak values during load transients are within 1% of the bus voltage (3 V). Bus voltage steady state is reached in less than 5 ms.

D. S3DCX: Output Series Connection—Voltage Regulation

Fig. 14 illustrates the operation of the regulator with the configuration represented in Fig. 11(right) under a step load of approximately 500 W. At the beginning, DCX 3 and DCX 4 are regulating the bus voltage and the load step forces the operation of DCX 5. It is important to note that DCX 3 and DCX 4 are accommodating 50 V solar sections and, DCX 5 at 100 V solar section, as it can be observed from the voltage measured in the resonant capacitor, C_r, of each DCX.

E. S3DCX: Output Series Connection—Unbalanced Solar Array Currents

The last results show the proper operation of the regulator with output series connection and unbalanced solar array currents. The regulator has been configured as represented in Fig. 11(right), but SAS 2 reduces its current to $I_{\mathrm{SC}} = 3.2$ A and $I_{\mathrm{MP}} = 3$ A. As depicted in Fig. 15, as the output current is limited, the operating point of the solar sections adjust to a value where both currents are equal. This effect is clearly shown in Fig. 16, where SAS 1 and SAS 2 exhibit different voltages, either during regulation or fully ON operation modes. It is also worth to note, that SAS 3 operates at the nominal value, since SAS 3 and SAS 4 are not unbalanced. Thus, it is important to remark that DCX

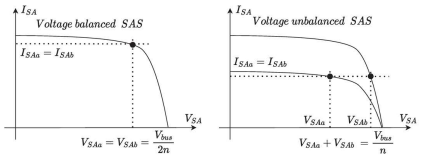

Fig. 15. Sketch of balanced and unbalanced solar array sections in output series connection.

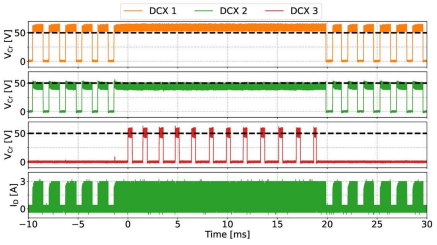

Fig. 16. S3DCX voltage regulation – output series connection and unbalanced solar array currents. Top: DCX 1: V_{Cr}; Middle Top: DCX 2: V_{Cr}; Middle Bottom: DCX 3: V_{Cr}; Bottom: DCX 1: I D_1.

output series connection is possible, with no loss of ZVZC conditions, even with unequal I-V curves of the solar array.

V. CONCLUSION

This article introduces a different concept for solar array regulation that solves some of the problems associated to direct energy transfer regulators commonly used in bus regulated satellites. The use of the proposed DCX topology provides two degrees of freedom for regulating bus voltage: transformer turns ratio, and output series connection of individual solar array sections, offering true adaptability to accommodate different types of solar arrays. Although this concept has been validated for a high voltage bus at 300 V, assuming step-up voltage conversion, other approaches are possible. Design example, computer simulation, and experimental prototype has been also included in this article to show the operating principles of the proposed regulator. Next steps include higher bus voltage (600 and 900 V), miniaturization of DCX increasing switching frequency (GaN power semiconductors and planar magnetics) and digital implementation (control and pulsewidth modulated gate signals).

APPENDIX

A. Design Guidelines: ZVZC Converter

1) Estimate the parasitic capacitance, C_p (2), from power semiconductors and transformer

$$C_M \approx 500\,\mathrm{pF}$$
$$C_{TR} \approx 300\ \mathrm{pF}$$
$$C_D \approx 100\ \mathrm{pF}$$

$$C_p = C_M + C_{TR} + C_D \cdot n^2 \approx 1.7 \text{ nF}. \quad \text{(A-1)}$$

2) Definition of the magnetizing current, i_m, as a percentage of the input current. An initial tentative of 20% of input current is considered. Low values i_m means larger transformers and longer t_{gap}, but lower transformer losses and better ZCS transitions

$$i_m = 0.2 I_{\text{SA}} = 0.8 \text{ A}. \quad \text{(A-2)}$$

3) Estimation of required gap time to charge the parasitic capacitance, t_{gap}, and estimation of ON time, t_{on}, as a percentage of t_{gap} to maximize power transfer. Estimation of switching frequency, f_s

$$t_{\text{gap}_{\text{min}}} > \frac{4 V_{\text{bus}} C_p}{i_m n} = 0.85 \ \mu\text{s} \quad \text{(A-3)}$$

$$t_{on} \approx \frac{t_{\text{gap}_{\text{min}}}}{0.3} = 2.85 \ \mu\text{s} \quad \text{(A-4)}$$

$$f_s = \frac{1}{2\left(t_{\text{on}} + t_{\text{gap}}\right)} = 135 \text{ kHz}. \quad \text{(A-5)}$$

4) Estimation of magnetizing inductance, L_m and transformer design

$$L_m = \frac{V_{\text{bus}} t_{\text{on}}}{2 i_m n} = 178 \ \mu\text{H}. \quad \text{(A-6)}$$

5) Transformer design. From the above inputs, a RM14/I core and 3C95 material with five turns ON primary, $n_1 = 5$, and 15 turns ON secondary, $n_2 = 15$ is considered. Measured values of five transformers will result in the following values (average of five measured transformers):

$$\begin{aligned} L_M &\approx 170 \ \mu\text{H} \\ C_{TR} &\approx 200 \text{ pF} \\ L_{lk} &\approx 650 \text{ nH}. \end{aligned} \quad \text{(A-7)}$$

6) Check if the transformer values are consistent with the original design and go back to step 1, if necessary.

7) Gap time, t_{gap}, calculation from measured values and using the following expressions:

$$\begin{aligned} &t_{\text{gap}} = \frac{1}{\omega_{\text{gap}}} \\ &\left(\arcsin\left[\frac{8 L_m \cos(\theta) C_p \omega_{\text{gap}}}{t_{\text{on}}} + \sin(\theta)\right] - \theta\right) = 0.9 \ \mu\text{s} \\ &\omega_{\text{gap}} = \frac{1}{\sqrt{L_M C_p}} \\ &\tan(\theta) = \frac{-2}{\omega_{\text{gap}} t_{\text{on}}}. \end{aligned} \quad \text{(A-8)}$$

8) Calculation of resonant frequency, ω_r, to satisfy zero current switching condition. Resonant frequency is found by numerical methods

$$\begin{aligned} &\cos(\omega_r t_{\text{on}}) - \omega_r \frac{t_{\text{gap}}}{2} \sin(\omega_r t_{\text{on}}) = 1 \\ &f_r = \frac{\omega_r}{2\pi} \approx 300 \text{ kHz}. \end{aligned} \quad \text{(A-9)}$$

9) Calculation of resonant capacitor, C_r

$$C_r = \frac{1}{\omega_r^2 L_{lk}} \approx 500 \ n\text{F}. \quad \text{(A-10)}$$

Design Guidelines: S3ZVZC MEA

10) Definition of maximum bus voltage ripple as per ECSS-E-ST-20C Rev.2, clause 5.7.2.m

$$\begin{aligned} &\Delta V_{\text{bus}|pp} < 0.5\% V_{\text{bus}} \\ &\Delta V_{\text{bus}|pp} = 1 \text{ V}. \end{aligned} \quad \text{(A-11)}$$

11) Definition of bus capacitance as per ECSS-E-ST-20C Rev.2, clauses 5.7.2.m and 5.7.2.o

$$C_{\text{bus}} = 400 \ \mu\text{F}. \quad \text{(A-12)}$$

12) Definition of MEA voltage reference, V_{ref}, and voltage feedback gain, K. V_{ref} is given by the internal voltage reference of the isolated error amplifier

$$V_{\text{ref}} = 1.225 \text{ V} \quad \text{(A-13)}$$

$$K = V_{\text{ref}} / V_{\text{bus}} = 4.083 \cdot 10^{-3}. \quad \text{(A-14)}$$

13) Definition of the hysteresis of the comparator and the transconductance of the regulator, G. Hysteresis voltage is selected as a function of the voltage supply rail and number of power cells. If the upper limit of the k cell is equal to the lower limit of the $k + 1$ cell, and the transformer turns ratio of all power cells are the same, n, the transconductance of regulator is simply the transconductance of one power cell

$$V_{Hi} - V_{Li} = V_{HL} = 1.2 \text{ V} \quad \text{(A-15)}$$

$$G = I_{SA} \ / \ (n \cdot V_{HL}) = 1.11 \text{ A/V}. \quad \text{(A-16)}$$

14) Calculation of proportional gain and integral term of the MEA, k_p and k_i, respectively, k_i is adjusted to be one decade below the crossover frequency of the voltage loop

$$k_p = \frac{V_{HL}}{K \Delta V_{\text{bus}|pp}} = 293.88 \quad \text{(A-17)}$$

$$k_i = k_p \ \frac{\omega_c}{10} = \frac{k_p^2 K G}{10 C_{\text{bus}}} = 97.96 \cdot 10^3 \text{s}^{-1}. \quad \text{(A-18)}$$

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Corrections

Corrections to "Sequential Switching Shunt Regulation Using DC Transformers for Solar Array Power Processing in High Voltage Satellites"

In [1], (A.7) and (A.8) are corrected as follows:

$$\begin{aligned} L_m &\approx 170\ \mu\text{H} \\ C_{TR} &\approx 200\ \text{pF} \\ L_{lk} &\approx 650\ \text{nH}. \end{aligned} \tag{A.7}$$

7) Gap time, t_{gap}, calculation from measured values and using the following expressions:

$$\begin{aligned} t_{\text{gap}} &= \frac{1}{\omega_{\text{gap}}} \cdot \left(\arcsin \left[\frac{8 L_m \cos(\theta) C_p \omega_{\text{gap}}}{t_{on}} + \sin(\theta) \right] - \theta \right) \\ &= 0.9 \mu\text{s} \\ \omega_{\text{gap}} &= \frac{1}{\sqrt{2 L_m C_p}} \\ \tan(\theta) &= \frac{-\sqrt{2}}{\omega_{\text{gap}} t_{\text{on}}}. \end{aligned} \tag{A.8}$$

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REFERENCE

[1] C. Orts, A. Garrigós, D. Marroquí, and A. Franke, "Sequential switching shunt regulation using DC transformers for solar array power processing in high voltage satellites," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 60, no. 1, pp. 421–429, Feb. 2024.

Received 4 November 2024; accepted 4 November 2024. Date of current version 6 December 2024.

DOI. No. 10.1109/TAES.2024.3492632

This work was supported by European Space Agency under Grant 4000136441/21/NL/GLC/my.

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3.3 Motivation

The main motivation for this article is to propose, design and validate a novel power processor for HV satellite bus, based on the inheritance of well-known solar array regulation techniques and DC-DC conversion topologies.

For decades, different SBSP-related initiatives have emerged worldwide. SOLARIS, which has been promoted and supported by ESA in Europe, is a notable example. The primary objective of this initiative is to lay the foundations for a space platform capable of generating photovoltaic power in the order of GW. A GW-scale platform would require a HV distribution bus in the range of tens of kV to minimize mass and DC losses in the distribution harness. These figures exceed existing space power systems by several orders of magnitude and pose a large number of challenges. Thus, this work aims to provide the first steps towards HV and high-power photovoltaic space power systems, starting from existing technology, that is power systems limited to tens of kW.

Briefly, two types of power architectures are typically implemented in a spacecraft, unregulated bus based on MPPT DC/DC converters and, regulated bus based on DET. Unregulated bus architectures are normally employed in low and medium power satellites operating in LEO orbits or interplanetary missions, where temperature and irradiance conditions vary considerably. In contrast, regulated bus is typically favoured in high power satellites in GEO, benefitting from more stable conditions over time. Considering the power levels and operating conditions contemplated for SBSP platforms, the S3R regulated bus seems the natural initial choice.

Increasing the voltage of solar arrays is the only way to provide a HV distribution bus for a space platform with DET power systems. At present, the voltage of the largest solar arrays is limited to 100 V-120 V. However, significant efforts are being made to boost solar array voltage up to 300 V or higher [10], [11], [12], [15], [41], [134]. However, this approach increases the risk of electrostatic discharge and electric arc formation between the solar cells due to the accumulation of electric charges on their surfaces [12]. Such discharges can damage or even destroy the solar cells, reducing the power generation capacity of the solar arrays. To minimize this risk, arc mitigation methods must be developed and implemented. Even with the development of this technology, HV solar arrays would need to undergo

validation and qualification to ensure their reliability in space environments. Alternatively, the voltage can be increased using a DC/DC converter while maintaining the 100 V – 120 V solar arrays, offering a more reliable and less costly solution with actual solar array technology.

Different converters can be used to achieve a HV distribution bus, as discussed in Chapter 2, with the DCX being the most suitable for this application due to its high efficiency, galvanic isolation, simplicity, and constant gain. A noteworthy topology is the current-fed push-pull Zero Voltage Zero Current (ZVZC) converter disclosed in [135] and thoroughly described in [125]. This topology is characterized by a resonant circuit formed between the transformer leakage inductance and a resonant capacitor in the circuit.

Based on the preceding analysis for a HV and high-power platform like SBSP, an architecture with low voltage solar arrays and regulated HV distribution is proposed. Therefore, a new solar array power processing system termed S3DCX, initially proposed in [136], [137] is suggested, combining S3R regulation method with a resonant DCX to elevate the voltage to the required level.

3.4 Article analysis

The proposed S3DCX is a solar array regulation technique designed for a HV distribution bus. It is composed of four main different parts: the SAS**,** where power is generated at a low voltage; the power cell, which steps up the voltage to match the requirements of the HV distribution bus; the MEA, which generates an error signal as part of the control loop to ensure proper regulation; and the HV-bus**,** which distributes the regulated HV and connects to the loads. A possible implementation of the S3DCX based on a push-pull DCX, is shown in Figure 23.

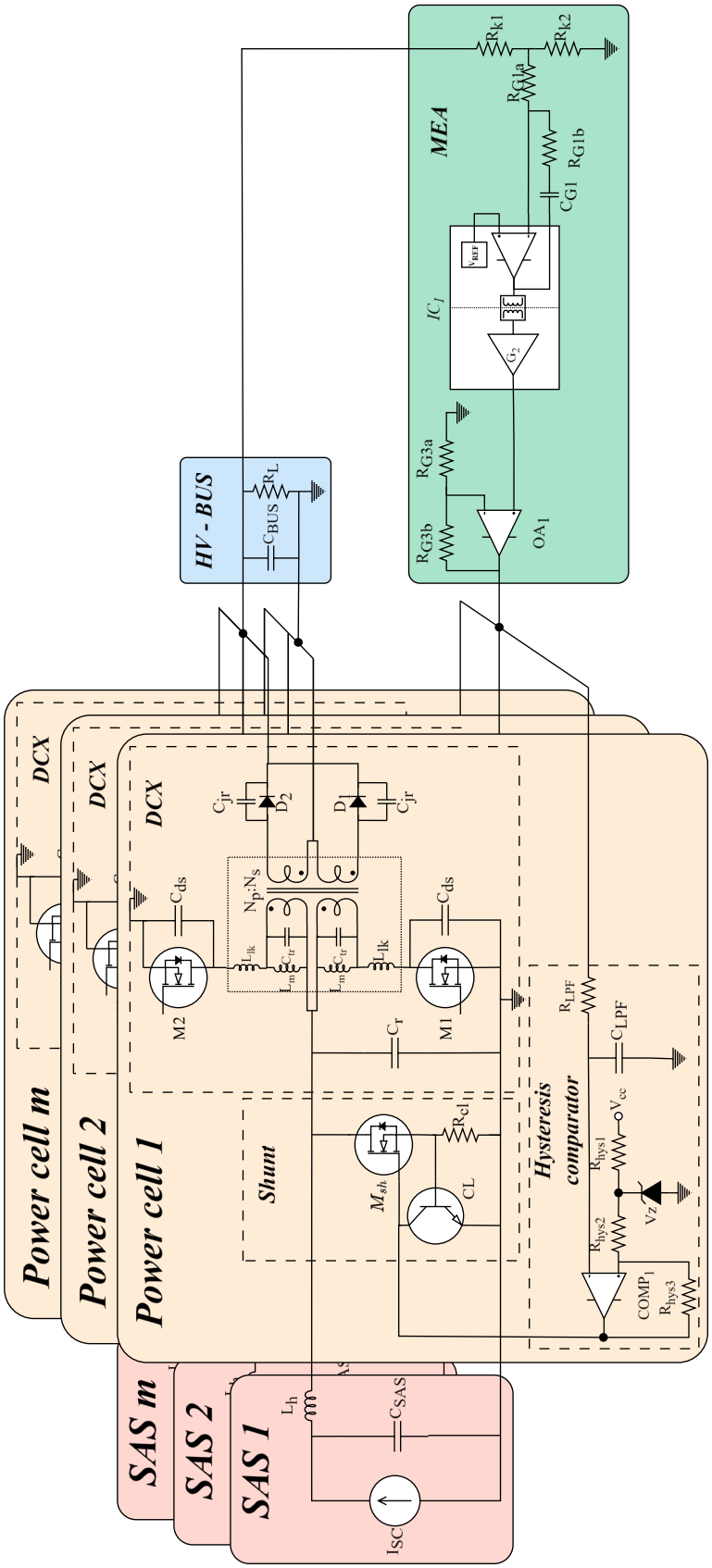

Figure 23. Schematic of the S3DCX regulator with a push-pull DCX. Extracted from [138].

The SAS can be modelled as a constant current source, I_{SC}, since it typically operates on the left side of the MPP. In a SAS, each solar cell has a non-linear junction capacitance whose value depends on factors such as the technology used, ambient conditions and whether the capacitance is charging or discharging due to shunt regulation [139]. The total parasitic capacitance of the solar array section can be simplified as a single capacitor, C_{SAS}. The SAS is connected to the power cell via a harness, which, in large satellites, can range from a few meters to hundreds of meters in length. Therefore, the equivalent harness inductance, L_h, must be taken into account in the analysis.

The power cell comprises three elements to achieve both regulation and voltage conversion. The first element is the DCX, which in this proposal, is implemented as a current-fed push-pull resonant ZVZC switching converter [125]. The operating principle of this converter can be described with the help of Figure 24. If either M_1 or M_2 is switched ON, i.e. during t_{on}, a resonant circuit appears between the transformer leakage inductance, L_{lk}, and the resonant capacitor, C_r and Zero Current Switching (ZCS) can be achieved by proper design of the resonant circuit elements and t_{on}. During t_{gap}, M_1 and M_2 are switched OFF, with the magnetising energy of the transformer being used to charge and discharge the parasitic capacitances, achieving the ZVS. The parasitic capacitances mainly include those of the switching MOSFETs, C_{ds}, the transformer, C_{tr}, and the diodes, C_{jr}. However, it should be noted that in practice, ZVZCS are not entirely achieved due to various effects [125]. The second element of the power cell is the low frequency switching shunt transistor and active current limiter [140], which prevents high current peaks during the SAS shunt caused by the discharge of C_{SAS} and C_r. The third element of the power cell is the hysteresis comparator, which commands the shunt transistor based on the error signal from the MEA. Additionally, a low-pass filter is included to eliminate the high frequency ripple from the DCX switching.

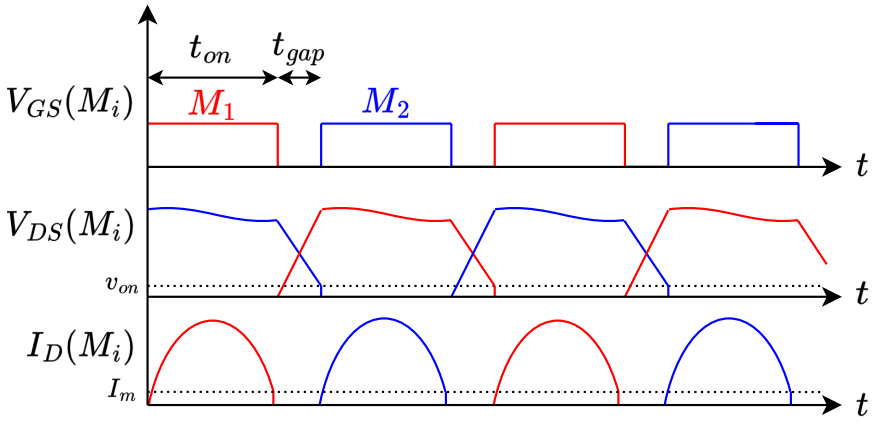

Figure 24. Sketch of the switching waveforms of the push-pull ZVZC converter

The MEA is implemented as a two-stage PI controller, incorporating a galvanically isolated operational amplifier that senses the HV distribution bus. The error signal is generated and distributed to all power cells, with the SAS connection and disconnection following the S3R concept [9]. The HV distribution bus is modelled as an output capacitance bus, C_{BUS}, and a variable resistive load, R_L, that represents the power consumption of the different loads. The control loop has been designed in accordance with the requirements of the ECSS-E-ST-20C [6] to meet static, dynamic and stability performance.

An experimental prototype of the S3DCX has been developed with five independent power cells, each one capable of processing 400 W from 100 V and 4 A SAS at nominal conditions and voltage gain N=3. The outputs of these power cells can be connected in series or parallel, depending on the desired bus voltage. The driving signals for the DCX MOSFETs and shunt MOSFET are provided by the internal analogic circuitry or from an external signal. A picture of the prototype is shown in Figure 25, and the schematics can be found in Annex I. The experimental validation is performed with the setup described in Annex II.

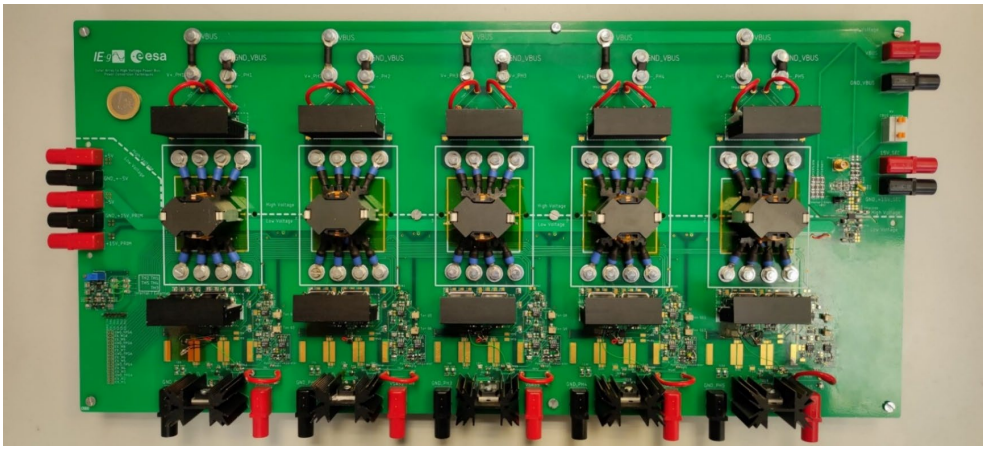

Figure 25. Five power cells S3DCX prototype.

3.4.1 S3DCX closed-control loop and dynamic response

The closed-control loop of the S3DCX resembles to a conventional S3R, with the key difference being the voltage and current gain introduced by the DCX. The sequential control of the power cells exhibits non-linear behaviour due to the influence of the hysteresis control. If each solar array generates the same amount of current, they can be linearised into a single controlled current source that is dependent on a voltage signal, as illustrated in Figure 26.(a). The equivalent transconductance gain, G, is defined by (**5**) and depends on the maximum current flowing to the bus, I_{bus}, that is the sum of the currents from each SAS, I_{SAS_i}, divided by the transformation gain of each DCX, n_i, and the voltage error signal range, V_C, which is determined by the hysteresis comparators.

$$G = \frac{I_{bus}}{V_C} = \frac{\sum_{i=1}^{m} I_{SAS_i}/n_i}{V_{Hm} - V_{L1}} \tag{5}$$

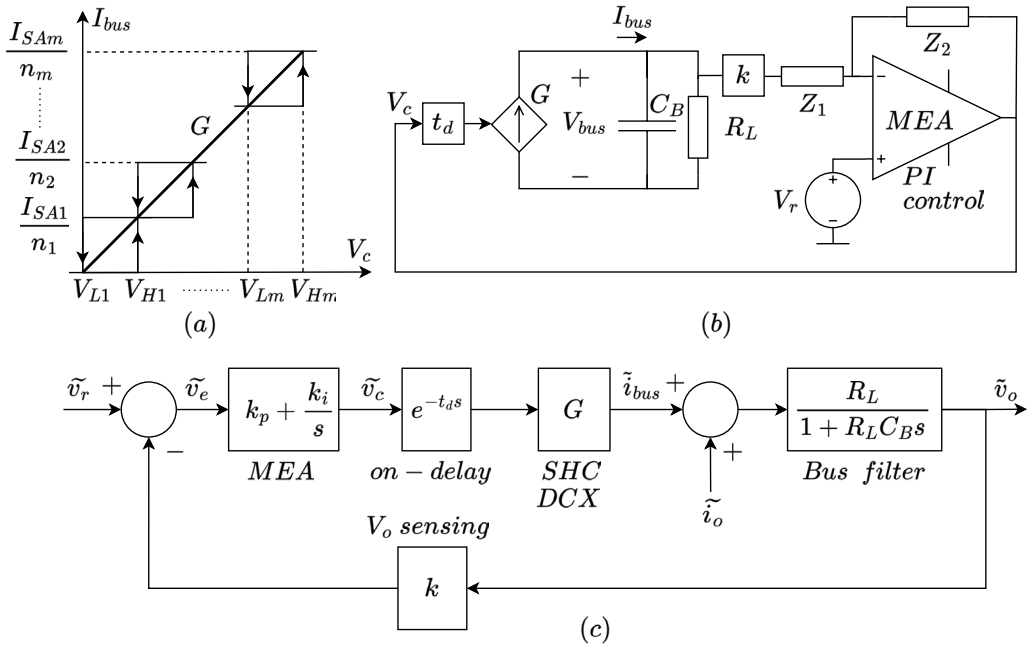

Figure 26. (a) Linearized sequential hysteresis control.
(b) Small-signal linear model. (c) Voltage feedback loop. Extracted from [132].

Once the power cells have been linearised, the S3DCX can be simplified into a small-signal linear model, as represented in Figure 26.(b). This model consists of the dependent current source, the bus capacitor, the resistive load, and the MEA. When a power cell is switched on, there is a delay, t_d, between the command generated by the signal error and the

actual operation that changes the state of the power cell. This delay can lead to phase margin degradation, which affects the stability of the control loop. This must be considered during the design process.

The block diagram of the small-signal linear model, Figure 26.(c), is used to analyse the dynamic response of the control loop. It is assumed that the delay is attributable to the time required to initiate power transfer from the solar array section to the main bus. The transfer function of a turn-on delay can be modelled using an exponential function, and the second-order Padé approximation is used to simplify the analysis. A further simplification, which still retains sufficient accuracy [141], consists of reducing to a first order numerator as defined in (**6**).

$$e^{-t_d s} \approx \frac{-2t_d s + 6}{t_d^2 s^2 + 4t_d s + 6} \tag{6}$$

The loop gain function is defined by (7), from which the poles and zeros can be identified as expressed in equation (8).

$$T_v(s) = kG\frac{k_p(s + k_i/k_p)}{s} \cdot \frac{1}{C_B\left(s + \frac{1}{R_L C_B}\right)} \cdot \frac{1 - s\,t_d/3}{s^2 t_d^2/6 \; + s\,2t_d/3 + 1} \tag{7}$$

$$\begin{aligned} Zeros{:}\ \omega_{PI} &= \frac{k_i}{k_p}\ ;\ \omega_{zd} = \frac{3}{t_d} \\ Poles{:}\ \omega_L &= \frac{1}{R_L C_B}\ ;\ \omega_d = \frac{\sqrt{6}}{t_d}\ ;\ \xi_d = \sqrt{6}/3 \end{aligned} \tag{8}$$

Therefore, the loop gain function can be rewritten in terms of poles and zeros (9), (10). Assuming the relationship between the different frequencies of the loop transfer function given by (11), the crossover frequency, ω_c, can be calculated (12), (13). It should be noted that this approximation is only valid if t_d satisfies (14).

$$T_v(j\omega) = \frac{kGk_p}{C_B} \cdot \frac{j\omega + \omega_{PI}}{j\omega} \cdot \frac{1}{j\omega + \omega_L} \cdot \frac{1 - \frac{j\omega}{\omega_{zd}}}{\left(\frac{j\omega}{\omega_d}\right)^2 + s2\xi_d/\omega_d + 1} \tag{9}$$

$$|T_v(j\omega)| = \frac{kGk_p}{C_B} \cdot \frac{\sqrt{\omega^2 + \omega_{PI}^2}}{\omega} \cdot \frac{1}{\sqrt{\omega^2 + \omega_L^2}} \cdot \frac{\sqrt{1 + \omega^2/\omega_{zd}^2}}{\sqrt{(1 - \omega^2/\omega_d^2)^2 + (2\xi_d\omega/\omega_d)^2}} \tag{10}$$

$$\omega_L < \omega_{PI} < \omega_{BW} < \omega_d < \omega_{zd} \tag{11}$$

$$|T_v(j\omega_{BW})| = \frac{kGk_p}{C_B} \cdot \frac{1}{\omega_{BW}} = 1 \tag{12}$$

$$\omega_c = \frac{kGk_P}{C_B} \tag{13}$$

$$t_d \ll \frac{\sqrt{6}}{4 \cdot \omega_{BW}} \tag{14}$$

The output impedance (15) of the regulator can be obtained from the block diagram shown in Figure 27.

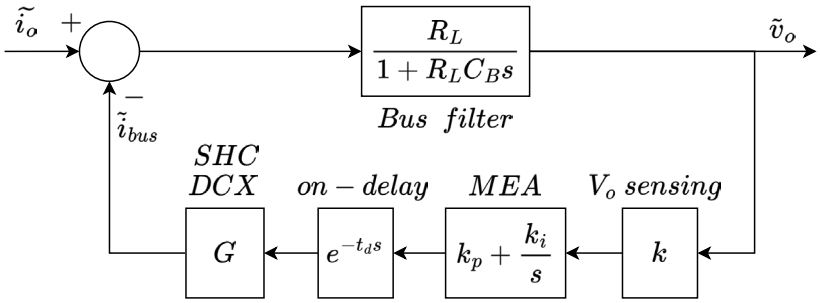

Figure 27. Output impedance feedback loop

According to the ECSS impedance mask, the maximum value of the impedance mask occurs within a frequency range of between 0,1 and 10 kHz, between ω_L and ω_c. The maximum value of the output impedance is defined as (16), and can be easily adjusted by modifying the proportional gain of the control loop, k_p.

$$Z_o(s) = \frac{1}{C_B} \cdot \frac{s(s + 1/t_d)}{s^3 + s^2\left(\frac{1}{t_d} + \frac{1}{C_B R_L}\right) + s\left(\frac{1}{C_B R_L t_d} + \frac{Gkk_p}{C_B t_d}\right) + \frac{Gkk_i}{C_B t_d}} \tag{15}$$

$$|Z_o(s)|_{max} = \frac{1}{Gkk_p} \tag{16}$$

The phase margin degradation produced by t_d is reflected in the output impedance as a peak close to the crossover frequency ω_c as shown in Figure 28. Thus, t_d must be limited as indicated in equation (14), to keep the output impedance within the mask limits.

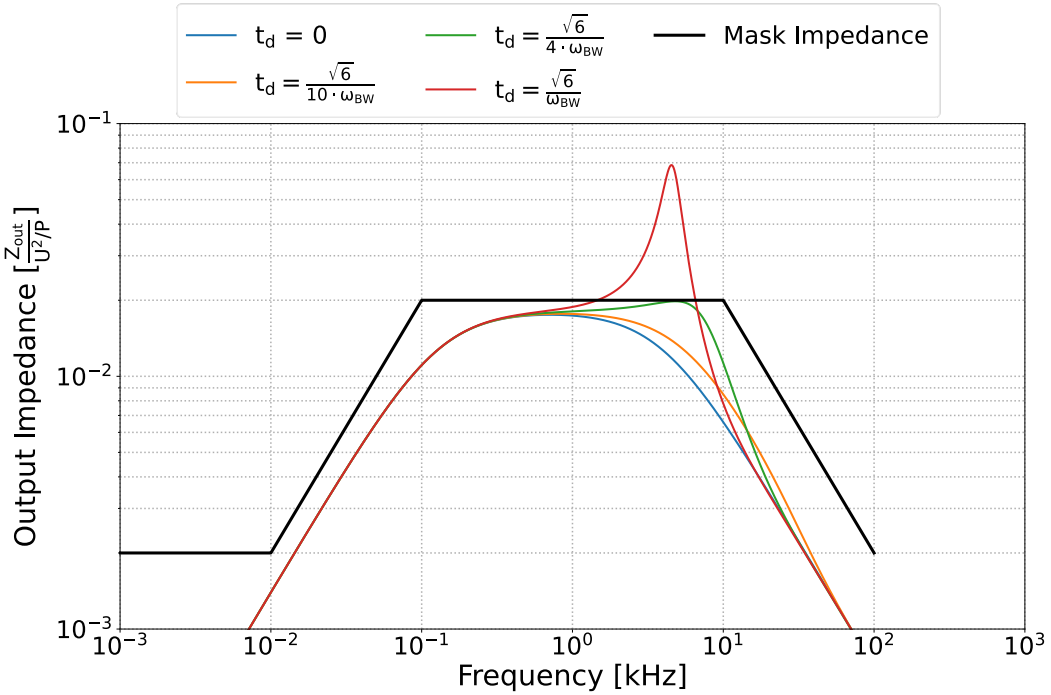

Figure 28. Normalized output impedance mask as a function of different values of turn-on delay

Two main factors contribute to the time delay, t_d, the turn-off time of the shunt MOSFET and the time required to charge C_{SAS} and C_r. As no power transfer occurs during this period, the equivalent circuit depicted in Figure 29 is applicable.

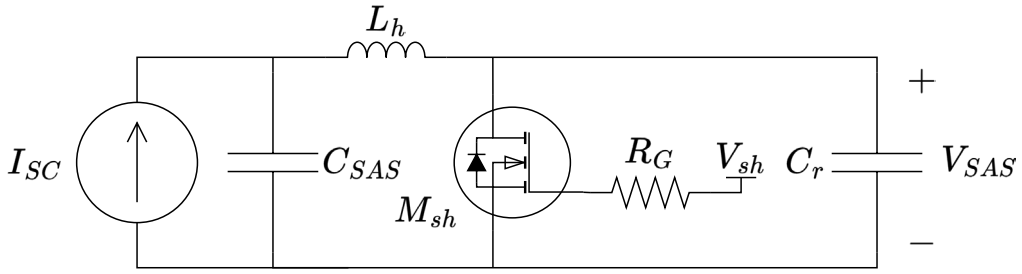

Figure 29. Equivalent circuit during turn-on switching of the power cell

As illustrated in Figure 30, the time delay, t_d, can be modelled in three stages. First, $t_{d_{on}}$, represents the discharge of the gate-source capacitance, C_{gs}, from the initial voltage V_{DRV}, to the Miller's voltage, V_{pla}, which is defined by equation (17). During the next interval, t_{d_m}, the drain-gate capacitance is discharged at a constant current rate determined by the gate

resistor, R_G, and V_{pla}, as represented by equation (18). The third interval, t_{d_C}, is the required time to charge the capacitances C_{SAS} and C_r, up to the regulated voltage of the solar panel, V_{SAS}, at which point the power cell begins transferring power to the bus, as defined in equation (19). Therefore, the total turn-on delay time is the sum of $t_{d_{on}}$, t_{d_m} and t_{d_C}. From a practical point of view, it can be considered that charging C_{SAS} and C_r takes much more time than turning off the shunt MOSFET, hence, $t_d \approx t_{d_C}$.

$$t_{d_{on}} = -R_g C_{gs} \ln\left(\frac{V_{pla}}{V_{DRV}}\right) \tag{17}$$

$$t_{d_m} = R_g \cdot \frac{Q_{gd}}{V_{pla}} \tag{18}$$

$$t_{d_C} = (C_r + C_{SAS}) \cdot \frac{V_{SAS}}{I_{SC}} \tag{19}$$

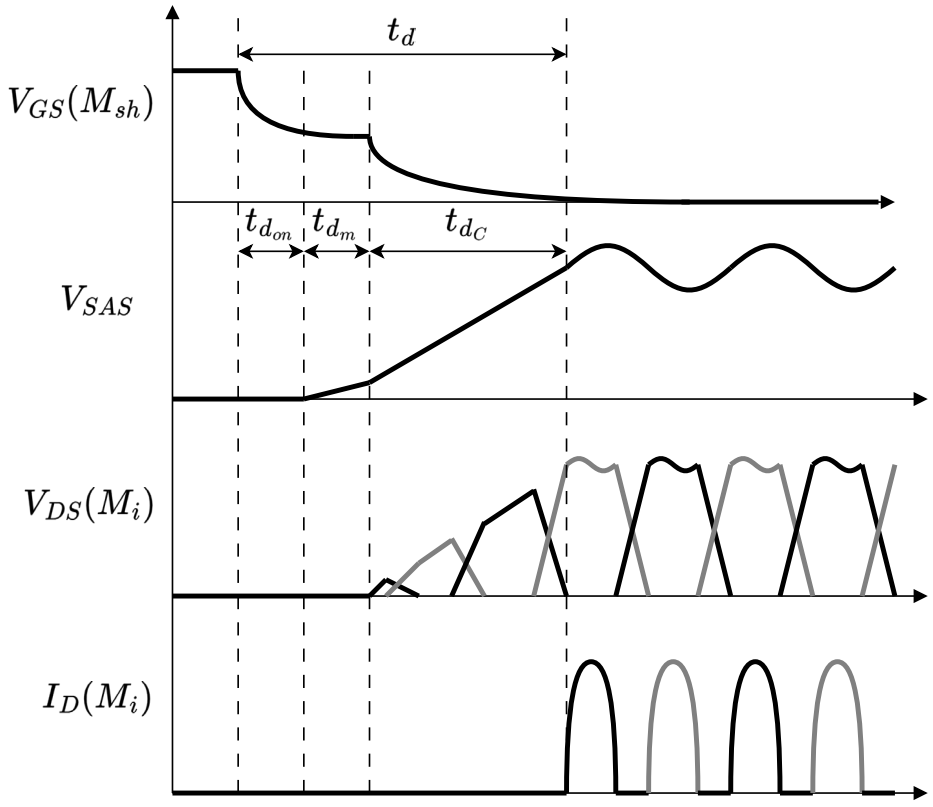

Figure 30. Sketch of the main waveforms during power cell turn-on.

Each individual contribution to the turn-on delay (20) has been estimated using the parameters listed in Table 6. This delay has also been verified through simulation in LTSpice

resulting in similar values, as shown in Figure 31. It is worth noting that the highest contribution in the delay is t_{d_C}.

$$t_{d_{on}} = 1{,}1\ \mu s;\ t_{d_m} = 1{,}0\ \mu s; t_{d_C} = 17{,}5\ \mu s$$
$$t_d = 19{,}6\ \mu s \tag{20}$$

As it can be observed from Figure 32, the measured turn-on delay times are very close to the theoretical and simulation values, $t_{d_{on}} = 1{,}1\ \mu s$, $t_{d_m} = 1{,}0\ \mu s$ and $t_{d_C} = 16{,}3\ \mu s$, resulting in a total delay of $t_d = 18{,}4\ \mu s$.

Table 6. Main power cell parameters for turn-on delay calculations

Description	Value	Comment
Isc	$4\ A$	
V_{SAS}	$100\ V$	Solar array simulator – Agilent E4351B
C_{SAS}	$0{,}2\ \mu F$	
L_h	$33\ \mu H$	Added inductance
C_r	$0.5\ \mu H$	CB182G0105J
R_g	$220\ \Omega$	
M_{sh}	IXTQ42N25P	$V_{pla} = 6{,}5\ V$ $V_{DRV} = 13\ V$ $C_{gs} = 6\ nF$ $Q_{gd} = 30\ nC$

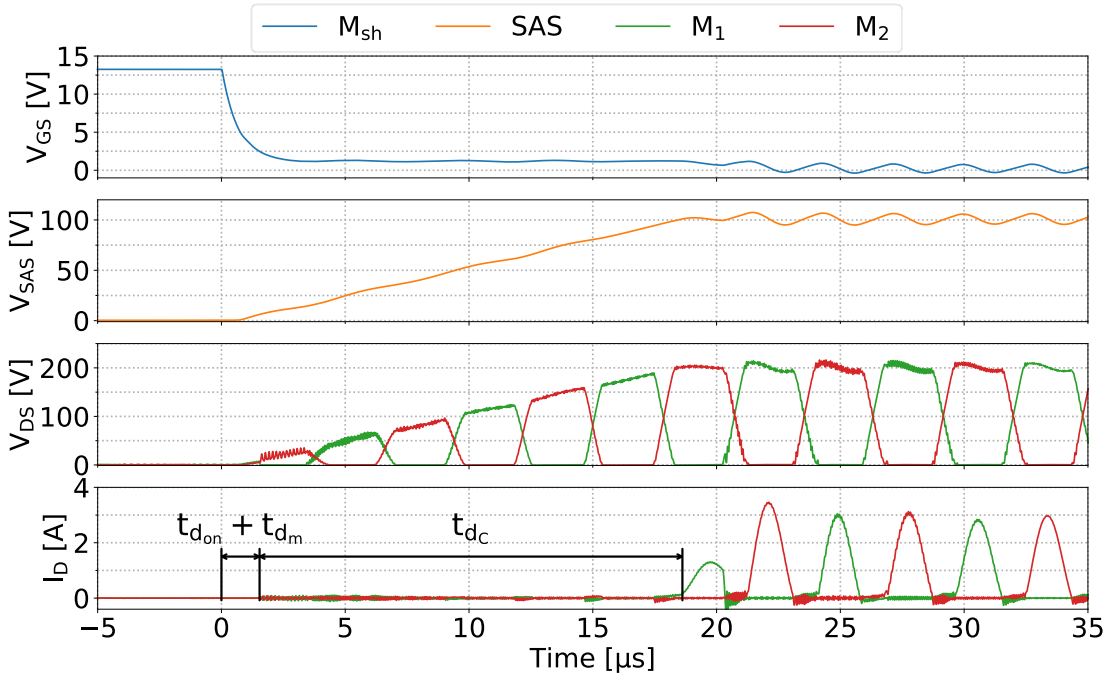

Figure 31. Simulation results of power cell turn-on transient. Top figure: Gate-source voltage of M_{sh}. Middle top figure: Solar array section voltage, V_{SAS}. Middle bottom figure: Drain-Source voltage of M_1 and M_2. Bottom figure: Output current of output rectifier diodes

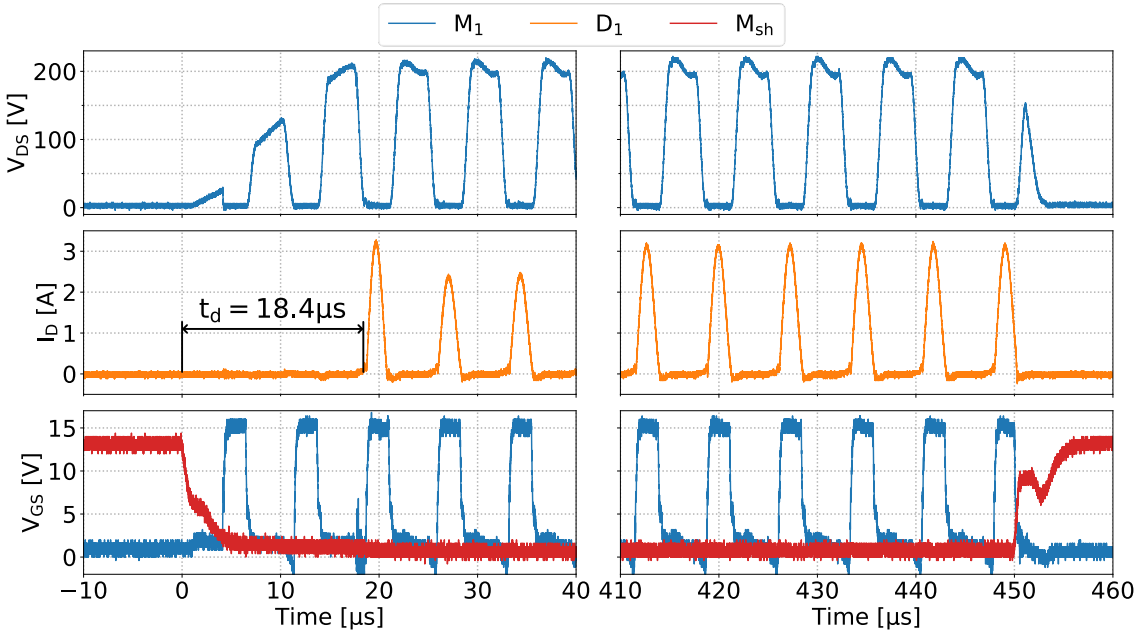

Figure 32. Left: DCX turn-on transient detail. Right: DCX turn-off transient detail. Top: Drain-Source voltage of M_1. Middle: Output current D_1. Bottom: Gate-Source voltage of M_1 and M_{sh}. Extracted from [132].

3.4.2 Design methodology

A design methodology for S3DCX has been developed, with the main objective of determining the circuit parameters that minimise the overall power losses. The methodology can be divided into two parts, in one side, the design of the DCX to meet the specifications and ZVZC switching conditions, and on the other side, the design of the control loop following the clauses of the standard ECSS-E-ST-20C [6] related to bus regulated systems. To achieve an optimal design of the DCX transformer, a software tool was developed to compute different solutions. The software was coded in *Python* and is available in Annex III.

The design process of the DCX, summarised in Figure 33, begins by defining the specifications for the S3DCX, including the input and output voltage. Together with the voltage specifications, some initial approximate component parameters are needed to start the design process. Specifically, for the MOSFETs, the on-resistance, r_{on}, and the parasitic output capacitance, C_M; for the output rectifier diodes, the forward voltage, V_f, and the junction capacitance, C_D; for the power transformer the parasitic capacitance, C_{TR}; and finally the dissipation factor, $\tan\delta$, for the resonant capacitor, C_r.

The design of the DCX is heavily influenced by the selected transformer, with the magnetizing current, I_m, being an important parameter. A large value of I_m allows for a reduction in the number of turns on the transformer and decreases the gap time, t_{gap}, allowing the increase of the switching frequency, f_{sw}. However, the downside of high I_m, is the power losses in the transformer and compromise the ideal conditions for ZCS. As there is no straightforward method to determine the optimal value of I_m, a range of possible values from 1 % to 25 % respect I_{SC} has been assessed.

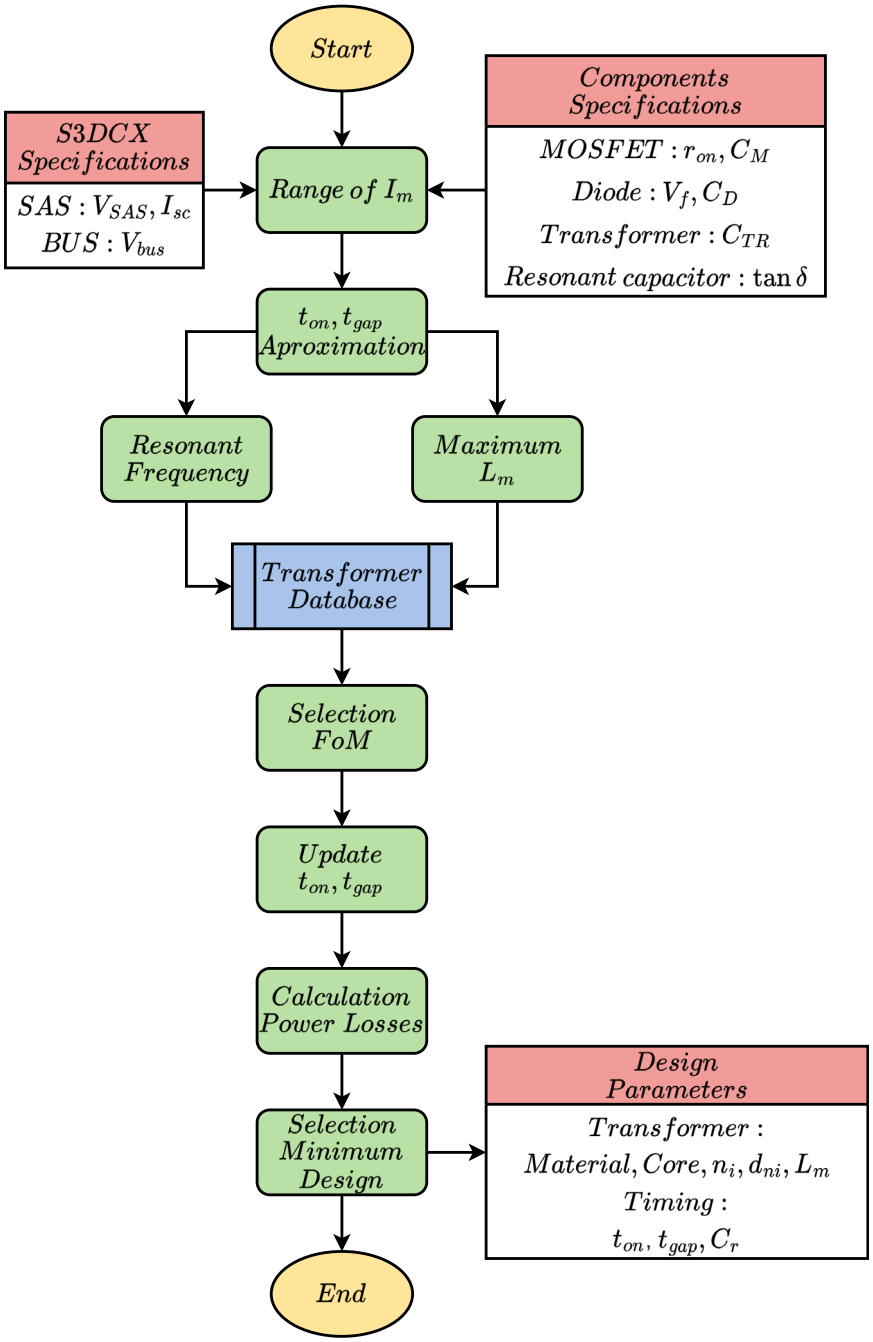

Figure 33. Design process for a theoretical DCX at minimum power losses.

One limiting factor to increase the f_{sw} is the required time, t_{gap}, to charge and discharge the parasitic capacitances, C_p, ensuring the ZVS. The value of C_p, which depends on the transformer turn ratio, N, can be estimated using equation (21).

$$C_p = C_M + C_{TR} + C_D N^2 \tag{21}$$

A first estimation of the minimum gap time, $t_{gap_{min}}$, can be calculated using (22), assuming the DCX is implemented in a push-pull topology, which doubles C_p, and assuming a constant current discharge based on the evaluated I_m. To ensure an efficient power transfer, t_{on} must be greater than $t_{gap_{min}}$. This can be approximated as a percentage of the duty cycle, D, ranging from 55 % to 90 % as defined in (23). The reasoning behind this range of values is that a low duty cycle would entail a low power transfer, while a high duty cycle would substantially reduce f_{sw}.

$$t_{gap_{min}} = \frac{4V_{SAS}C_p}{I_m} \tag{22}$$

$$t_{on} = t_{gap_{min}} \frac{D}{1-D} \tag{23}$$

Knowing t_{on}, the maximum magnetising inductance, $L_{m_{max}}$, is determined by (24). Now, a list of potential transformers can be created from $L_{m_{max}}$, but before, the resonant frequency, ω_r, that fulfils the ZCS must be calculated to account for the conduction losses. The value of ω_r is obtained through numerical methods from the transcendental equation (25). In addition, during the t_{on}, the resonant current follows (26) and the Root Mean Square (RMS) current, I_{rms}, can be calculated by applying (27) and (28).

$$L_{m_{max}} = \frac{V_{SAS}t_{on}}{2I_m} \tag{24}$$

$$\cos(\omega_r t_{on}) - \omega_r \frac{t_{gap}}{2} \sin(\omega_r t_{on}) = 1 \tag{25}$$

$$\mathrm{i_r(t)} = I_{SAS}\left(1 - \frac{\cos(\omega_r t + \varphi)}{\cos(\varphi)}\right) \tag{26}$$

$$\tan\varphi = \omega_r \frac{t_{gap}^2}{t_{on} + t_{gap}} \tag{27}$$

$$I_{rms} = \sqrt{\frac{1}{t_{on} + t_{gap}} \int_0^{t_{on}} i_r^2(t)\, dt}$$

$$I_{rms} = I_{SAS} \sqrt{\frac{1}{t_{on} + t_{gap}} \left(t_{on} + \frac{t_{on}}{2\cos^2 \varphi} + \frac{3 \tan \varphi}{\omega_r} \right)} \tag{28}$$

The duty cycle significantly influences the I_{rms} value, directly impacting on the conduction losses. As shown in Figure 34, an optimal I_{rms} value is attained with a duty cycle of approximately 80 %.

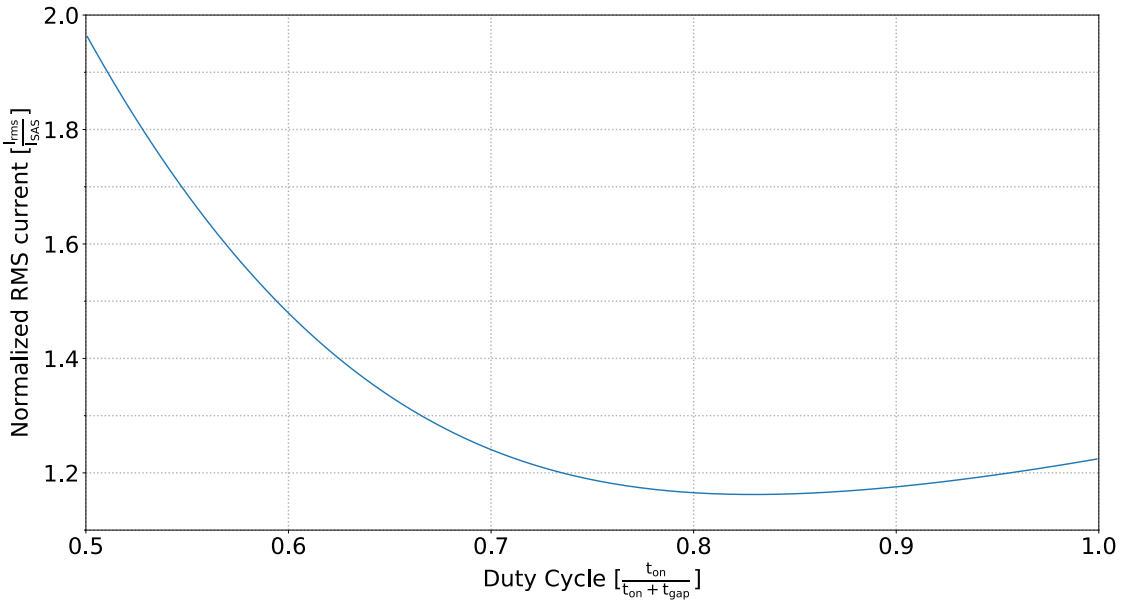

Figure 34. Normalised I_{rms} respect I_{SAS} as a function of the duty cycle.

Using the previous parameters and defining the winding factor, w_{ff}, and the maximum current density in the windings, J_{max}, a search of commercially available magnetic cores is conducted in a database. This database includes information of the core geometry and magnetic properties, generating a list of suitable transformers for each value of I_m. The complete design process, along with the calculation involved, is detailed in section 3.4.3.

To select the most suitable transformer previously computed for each value of I_m, a Figure of Merit (FoM) is defined. This FoM evaluates the transformers in terms of power losses, P_{TR}, and mass, m_{TR}, as defined in (29). The algorithm provides a final classification, and the selected transformers will be the ones that provide the minimum FoM value.

$$FoM = P_{TR} \cdot m_{TR} \tag{29}$$

Now, t_{gap} is recalculated using the actual L_m according to equations (30), (31) and (32).

$$\omega_{gap} = \frac{1}{\sqrt{2L_m C_p}} \tag{30}$$

$$\tan\theta = \frac{-\sqrt{2}}{\omega_{gap} t_{on}} \tag{31}$$

$$t_{gap} = \frac{1}{\omega_{gap}} \left[\arcsin\left(\frac{8L_m \cos\theta \, C_p \omega_{gap}}{t_{on}} + \sin\theta\right) - \theta\right] \tag{32}$$

Next, with the updated t_{gap}, the resonant frequency, ω_r, is recalculated using (25). The resonant frequency, ω_r, is a function of the transformer leakage inductance, L_{lk}, the harness inductance, L_h, and C_r, as defined in (33). Assuming that $L_h \gg L_{lk}$, the equation (33) can be simplified and rearranged to calculate the value of C_r to ensure the ZCS condition (34).

$$\omega_r = \sqrt{\frac{L_h + L_{lk}}{L_h L_{lk} C_r}} \tag{33}$$

$$C_r = \frac{1}{L_{lk} \, \omega_r^2} \tag{34}$$

During the gap time, C_r is charged with I_{SAS}, while C_p is discharged with I_m. Due to the impedance difference between these two circuit sections, minimal current flows between them, resulting in a voltage difference caused by the charge of C_r. This voltage difference is observed during the parasitic discharges in V_{DS} when it reaches its minimum value, v_{on}, thereby preventing it from reaching zero voltage. For a push-pull DCX topology, the value of v_{on} can be calculated using (35). A high value of v_{on} compromises the ideal waveform conditions and introduces large voltage steps during the turn-off, but, in practice, its magnitude remains small compared to V_{SAS}.

$$v_{on} = 2 \cdot \frac{I_{SAS} t_{gap}^2}{C_r (t_{on} + t_{gap})} \tag{35}$$

Once C_r is obtained, the design of the DCX is completed for each I_m evaluated. Now, to compare each individual design, converter power losses, P_t, are estimated. The evaluation of power losses is simplified to the resonant capacitor losses, P_{Cr}, the MOSFETs conduction losses, P_{cond}, the rectifier diodes conduction losses, P_d, and the transformer power losses, P_{Tr}. Switching losses on the MOSFETs and diodes have been neglected due to ZVS and ZCS. A complete explanation of the power losses calculation is provided in section 3.4.4.

Using the proposed design methodology, three options have been selected and compared, as represented in Figure 35 and summarised in Table 7. Option A) exhibits the highest efficiency but utilises the heaviest transformer. Conversely, option C) offers the lowest FoM, thus making it the preferred choice as it offers the optimal compromise between efficiency and transformer mass.

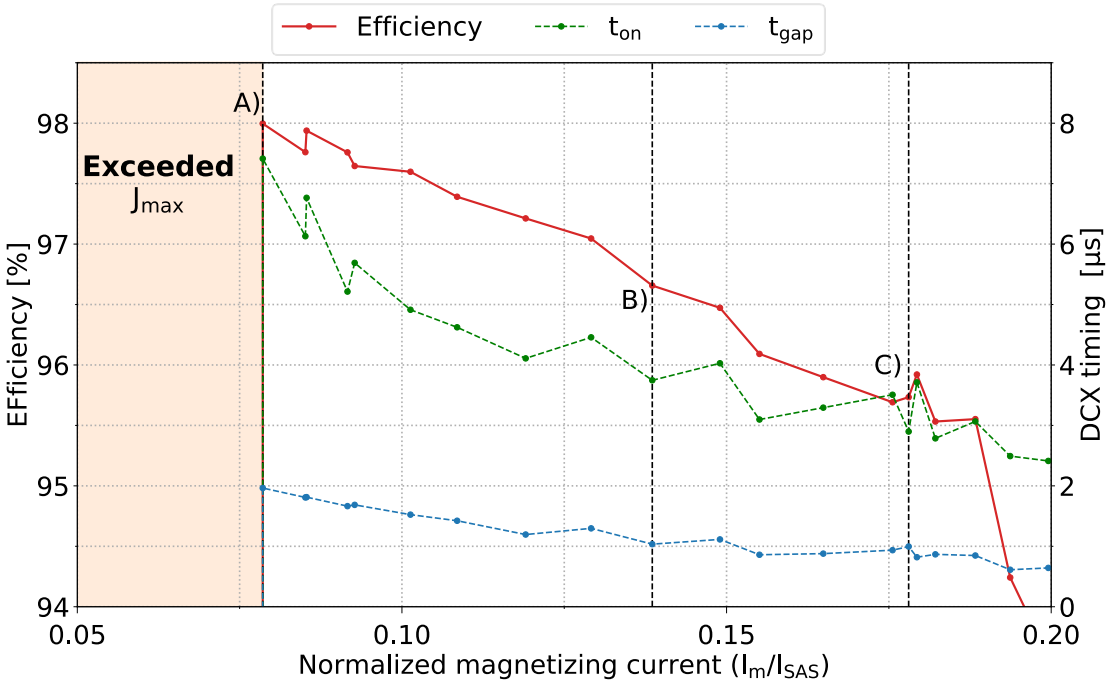

Figure 35. Theoretical efficiency and DCX timing ($\boldsymbol{t_{on}}$, $\boldsymbol{t_{gap}}$) vs the normalized value of $\boldsymbol{I_m/I_{SAS}}$.

Table 7. Summary of the theoretical design parameter for the selected DCX designs.

Design	A)	B)	C)
Core	E55	E42	RM14
Material	3C95	3C95	3C95
$L_m\ [\mu H]$	1.180	338	203
$N_1 : N_2$	12:36	8:24	5:15
$d_1\ [mm]$	1,75	2,00	1,82
$d_2\ [mm]$	1,00	1.16	1,05
$J\ [A/mm^2]$	1,94	1,47	1,6
$t_{on}\ [\mu s]$	7,4	3,7	2,8
$t_{gap}\ [\mu s]$	2,0	1,0	0,9
$f_{sw}\ [kHz]$	53	106	135
$C_r\ [\mu F]$	5,0	1,5	0,8
$\eta\ [\%]$	98,0	96,7	95,5
$m_{Tr}\ [g]$	290	130	90

Once the DCX design is complete, the transformer is implemented and characterised. Based on the measured values, a second iteration of the ZVZC condition is performed, with the objective of adjusting t_{gap} and C_r according to equations (32) and (34), respectively. The second iteration design process is summarised in Figure 36.

The second part of the design methodology involves establishing the parameters of the MEA and the hysteresis comparator that are integral part of the S3R control loop, ensuring the bus voltage meets the requirements of the ECSS-E-ST-20C [6]. The design procedure can be found in the annex of the published paper [132].

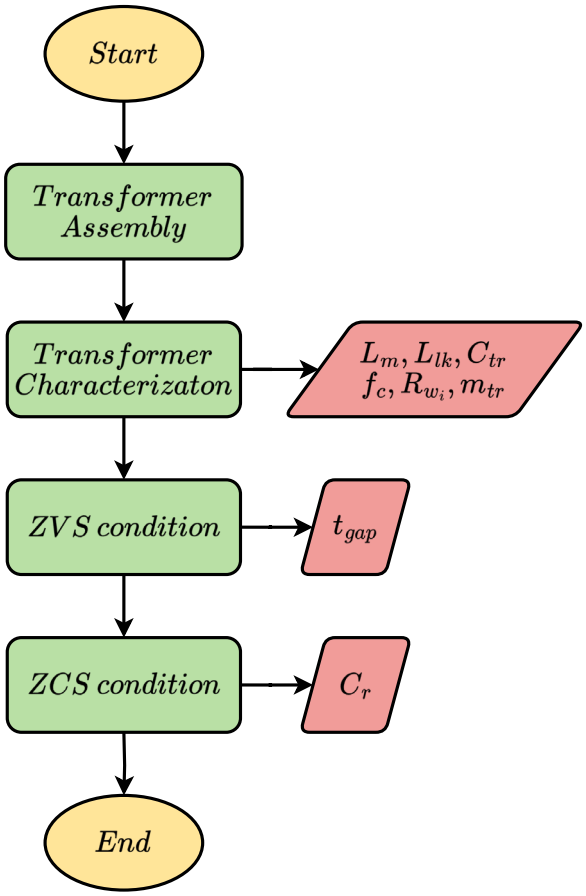

Figure 36. Design process flowchart for the second iteration: after transformer implementation.

3.4.3 Design and characterization of DCX transformers

The transformer has a significant impact on the overall mass, volume, and power losses of the DCX, and its parasitic elements affects the switching and resonant frequency. Consequently, transformer design constitutes a fundamental aspect of the system. The methodology employed for transformer design and construction is hereby presented. The study has been delimited to the push-pull topology using a database of commercially available magnetic core materials, and no toroidal cores have been considered.

The database is divided into two parts. The first part of the database includes the mechanical core information, the effective volume, V_{eff}, the effective length, l_{eff}, the effective area, A_{eff}, the winding length, l_w, the winding area, A_w, and the mass core, m_c. The second part of the database contains information regarding magnetic properties,

Steinmetz's coefficients, k_h, α, β; saturation flux density, B_s, relative magnetic permeability, μ_r, and the range of working frequencies, f_{min}, f_{max}.

Given the specified L_m and N, the number of turns, n_p, and n_s, are calculated for each combination of cores, as expressed in (36). It should be noted that some transformers may be invalid due to magnetic core saturation, which is checked using equation (37). If the calculation exceeds B_s, the transformer is then discarded from the selection process.

$$n_p = \sqrt{\frac{L_m l_{eff}}{\mu_o \mu_r A_{eff}}} \; ; n_s = \frac{n_p}{N} \tag{36}$$

$$B_s > B_{max} = \frac{V_{SAS} t_{on}}{n_p A_{eff}} \tag{37}$$

After determining the number of windings turns, the wire diameter is selected to minimise electrical resistance and, consequently, conduction losses. The available winding area is maximised while adhering to the maximum allowable current density, J_{max}, in the windings. For a push-pull transformer with four windings, a winding factor, w_{ff}, of 0.3 and J_{max} of 3 A/mm^2 are considered as the design criteria. The minimum required area for the winding wire, A_{Ji}, is then determined based on J_{max} as stated in (38). To ensure uniform conduction losses to favour thermal management, the winding wire areas at the primary, A_{J1}, and secondary, A_{J2}, are related as defined in (39).

$$A_{Ji} = \frac{I_{n_{rms}}}{J_{max}} \tag{38}$$

$$\frac{A_{J2}}{A_{J1}} = \frac{1}{N} \tag{39}$$

The minimum required winding area, A_{wJ}, is calculated based on the area for each winding wire, as defined in equation (40). The calculated area is then evaluated against the available space, A_w to determine if the windings fit within the transformer core, as stated in (41). If the available winding area of the transformer is found to be inadequate, the design is then excluded from the selection process.

$$A_{wJ} = \frac{2 \cdot (n_1 A_{J1} + n_2 A_{J2})}{wff} \tag{40}$$

$$A_w \geq A_{wJ} = \frac{4 n_1 A_{J1}}{wff} \tag{41}$$

In certain instances, the winding area obtained is considerably smaller than A_w, resulting in inadequate transformer utilisation. To address this, the available space is utilised by increasing the winding wire area, ΔA_1, thereby optimising conduction losses, as calculated in (42). Subsequently, the wire diameters for the primary winding, d_{n1}, and the secondary winding, d_{n2}, are calculated by (43) and (44), respectively.

$$\Delta A_1 = \frac{A_w - A_{wJ}}{2(1 + \frac{1}{N})} \tag{42}$$

$$d_{n1} = \sqrt{\frac{4}{\pi}(A_{J1} + \Delta A_1)} \tag{43}$$

$$d_{n2} = \frac{d_{n1}}{\sqrt{N}} \tag{44}$$

After determining the winding diameters, a comprehensive list of suitable transformers based on the initial design specifications is obtained. For the experimental prototype of the S3DCX, a RM14-3C95 transformer with a turn ratio of 5:15 has been selected. The final transformer must meet three key requirements. Firstly, it must provide more than 1,2 kV of electric isolation between the windings, in order to comply with the 50 % voltage derating requirement of the ECSS-Q-ST-30-11C [33]. Secondly, the variation of L_{Lk} between winding pairs must have less than 8 % of difference to ensure ω_r does not deviate more than 2% between switching cycles. Lastly, to minimise power losses due to the skin effect, the wire diameter must be smaller than 0.17 mm, considering a baseline switching frequency of 150 kHz.

In order to achieve the required electric isolation, it is necessary to introduce a polyamide layer, such as Kapton tape with a dielectric strength of 7 kV, between the transformer windings. With a switching frequency in the range of thousands of kHz, the use of Litz wire,

with each individual wire having a diameter of 71 µm, will reduce the skin effect losses. Nevertheless, ensuring equivalent L_{Lk} between winding pairs is non-trivial. As illustrated in Figure 37,four different winding distribution schemes have been assembled and tested for a RM14 core with an equal number of turns, in order to identify the optimal solution.

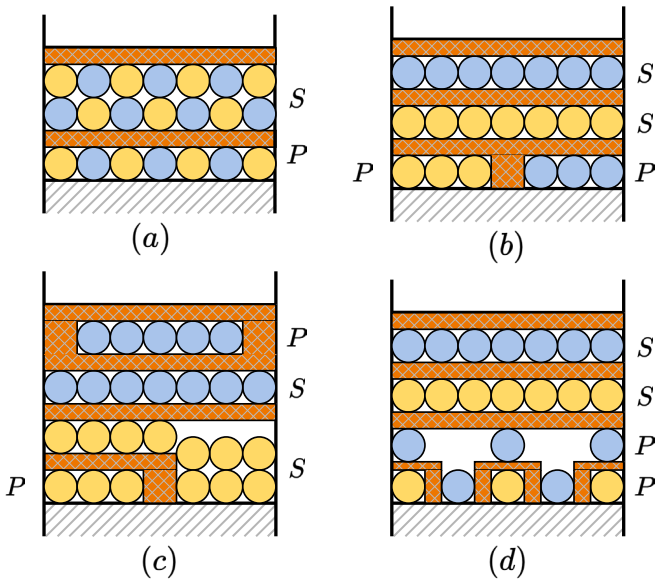

Figure 37. Four types of winding distribution tested for a push-pull transformer.

The measurement of transformer parameters, based on the electrical model depicted in Figure 38, has been conducted by employing the Bode 100 vector network analyser [142]. The L_m is determined through the measurement of one primary winding, while maintaining all other windings in an open circuit. This procedure is then repeated for the L_{lk} but with the respective secondary winding short-circuited.

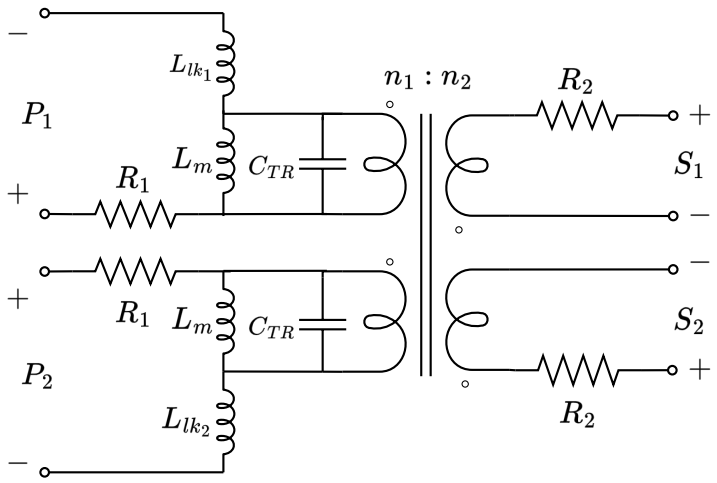

Figure 38. Electrical model for a four windings push-pull transformer. Extracted from [132].

The characterisation of transformers with the different winding strategies presented in Figure 37, is summarised in Table 8. Option (a) exhibits the lowest L_{lk}, which has been achieved by twisting the primary and secondary windings in pairs, but it must be discarded as it does not include the Kapton layer between the windings. Of the remaining three options, the transformer with winding distribution (d) is the preferred because it shows the lowest leakage inductance dispersion, ΔL_{lk}.

Table 8. Electrical parameters for various winding distribution for a RM14-3C95 transformer.

Parameters	(a)	(b)	(c)	(d)
$L_{m_1}\ [\mu H]$	171,0	177,1	176,0	160,2
$L_{m_2}\ [\mu H]$	171,0	177,7	175,7	160,3
$L_{lk_1}\ [nH]$	300	799	855	405
$L_{lk_2}\ [nH]$	267	937	1200	421
$\Delta L_{lk}\ [\%]$	11,0	14,7	28,8	3,8
$C_{TR}\ [pF]$	380	160	309	230

Subsequently, the option (d) was selected for implementation in the five DCX transformers. To ensure efficient assembly and replacement in the S3DCX prototype board, the winding wires were soldered to a ring terminal. The final assembly of one of the transformers is shown in Figure 39. Each transformer has been characterised, and their electrical parameters are listed in Table 9.

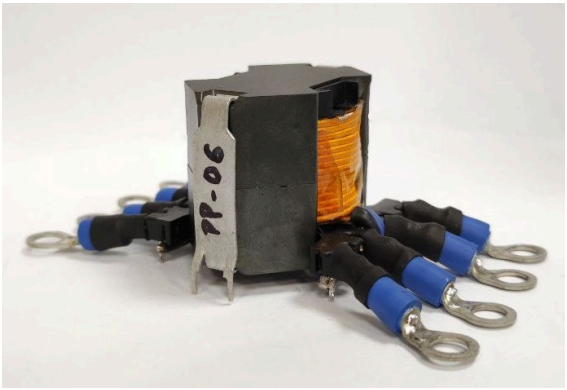

Figure 39. Fully assembled RM14-3C95 push-pull transformer with (d) distribution.

Table 9. Electrical parameters of the transformers implemented for the S3DCX prototype.

Parameters	DCX_1	DCX_2	DCX_3	DCX_4	DCX_5
L_{m_1} $[\mu H]$	172,8	174,4	168,3	168,7	165,1
L_{m_2} $[\mu H]$	172,8	174,5	169,7	168,9	165,1
L_{lk_1} $[nH]$	382	400	451	346	347
L_{lk_2} $[nH]$	400	357	405	368	369
C_{TR} $[pF]$	235	118	120	108	142
f_{res} $[kHz]$	789	830	925	962	874
R_{P1} $[m\Omega]$	9,6	8,0	8,7	8,5	9,2
R_{P2} $[m\Omega]$	13,0	9,1	9,3	11,8	13,1
R_{S1} $[m\Omega]$	38,7	40,9	37,5	40,7	39,9
R_{S2} $[m\Omega]$	42,7	38,3	41,6	41,2	41,9

3.4.4 Efficiency and power losses breakdown

Each DCX component contributes to a greater or lesser extent to the overall power losses, and it is important to know and analyse each contribution to improve the overall efficiency of the DCX. Theoretical power losses calculations have been compared to the experimental measurements. The main parameters and part references of the DCX are listed in Table 10.

The resonant capacitor C_r provides the AC current which can be high enough to result in noticeable power losses. The resonant capacitor current, i_{Cr}, is given by (45), where i_r is the resonant current that flows to the transformer (26). The RMS value of the current supplied by the resonant capacitor, $I_{Cr_{rms}}$, is given by (46), and resonant capacitor power losses by (47).

Table 10. S3DCX Main DCX design parameters for power losses calculations.

Description	Value	Comment
SAS – Agilent E4351B simulator		
I_{SC}	$4\ A$	Short-circuit current
V_{SAS}	$100\ V$	Voltage regulation point
DCX transformer – push-pull		
Core	RM14	$V_{eff} = 13{,}9\ cm^3; A_{eff} = 1{,}98\ cm^2$ $l_w = 71\ mm$
Material	3C95	$k_h = 92{,}166; \alpha = 1{,}045; \beta = 2{,}44$
$n = n_2/n_1$	15/5	$d_{n1} = 1{,}42\ mm; d_{n2} = 1\ mm$
L_m	$169{,}86\ \mu H$	Average value from implemented transformers
L_{lk}	$385{,}18\ nH$	
Relevant DCX parameters		
C_r	$0{,}5\ \mu F$	Ref: CB182G0105J $\tan\delta = 0{,}5\ \%; \omega_r = 1{,}61 \cdot 10^6\ rad/s$
$M_1; M_2$	IXTQ42N25P	Si MOSFET (250V, 42A) $r_{on} = 67{,}2\ m\Omega; C_{ds} = 350\ pF$
$D_1; D_2$	STPSC10H12	SiC diode (1.2kV, 10A) $V_f = 0{,}9\ V; R_d = 0{,}4\ \Omega$
t_{on}	$2{,}8\ \mu s$	$f_{sw} = 135{,}14 kHz; D = 0{,}7568$
t_{gap}	$0{,}9\ \mu s$	

$$i_{Cr}(t) = I_{SAS} - i_r(t) \tag{45}$$

$$I_{Cr_{rms}} = I_{SAS}\sqrt{\frac{1}{t_{on}+t_{gap}}\cdot\left(\frac{t_{on}}{2\cos^2\varphi}+t_{gap}-\frac{\tan\varphi}{\omega_r}\right)} = 3{,}2\ A \tag{46}$$

$$P_{Cr} = I_{Cr_{rms}}^2 ESR = I_{Cr_{rms}}^2 \frac{\tan\delta}{\omega_r C_r} = 46\ mW \tag{47}$$

M_1 and M_2 conduction losses, P_{cond}, are estimated by (48). Since DCX operates under ZVZCS conditions, switching and driving losses have been considered negligible.

$$P_{cond} = I_{rms}^2 r_{on} = 2{,}13\ W \tag{48}$$

Diode power losses, P_d, can be estimated using equations (49) and (50). Given that diodes also operate under the ZVZCS conditions, switching losses can also be disregarded.

$$I_{avg} = \frac{I_{SC}}{t_{on}+t_{gap}}\left(t_{on}+\frac{2\tan\varphi}{\omega_r}\right) = 3{,}5\ A \tag{49}$$

$$P_d = \left(\frac{I_{rms}}{N}\right)^2 R_d + V_F\frac{I_{avg}}{N} = 2{,}05\ W \tag{50}$$

The transformer power losses are divided into copper losses and core losses. Copper losses, $P_{w_{ni}}$, are estimated based on the DC resistive losses of the winding by (51). Hysteresis core losses, P_{hys}, are estimated through the Steinmetz's equation (52). The total transformer power losses, P_{Tr}, are then computed by summing both contributions using (53).

$$P_{w_{ni}} = \frac{4\rho_{Cu} n_i l_w I_{rms_{ni}}^2}{\pi d_{n_i}^2} = \begin{cases} P_{w_{n1}} = 83\ mW \\ P_{w_{n2}} = 57\ mW \end{cases} \tag{51}$$

$$P_{hys} = V_{eff} k_h f_{sw}^{\alpha} B_{max}^{\beta} = 13{,}52\ W \tag{52}$$

$$P_{Tr} = 2\cdot\left(P_{w_{n1}} + P_{w_{n2}}\right) + P_{hys} = 13{,}80\ W \tag{53}$$

The theoretical efficiency of the power cell rated at 400 W, operating the SAS at 100 V and 4 A, has been calculated to be 95,49 % by summing the individual contributions. The converter efficiency has been measured in each DCX from 1 A to 4 A of the input current, as shown in Figure 40. The maximum efficiency at 4 A is observed in DCX_1 and DCX_2,

achieving a value of 95,80 %, while the minimum efficiency measured was in DCX_4 , resulting in 95,10 %. The mean value of all DCX efficiencies is 95,48 %, which closely matches the theoretical efficiency.

$$P_{DCX} = P_{Cr} + P_{cond} + P_d + P_{Tr} = 18{,}03\ W \tag{54}$$

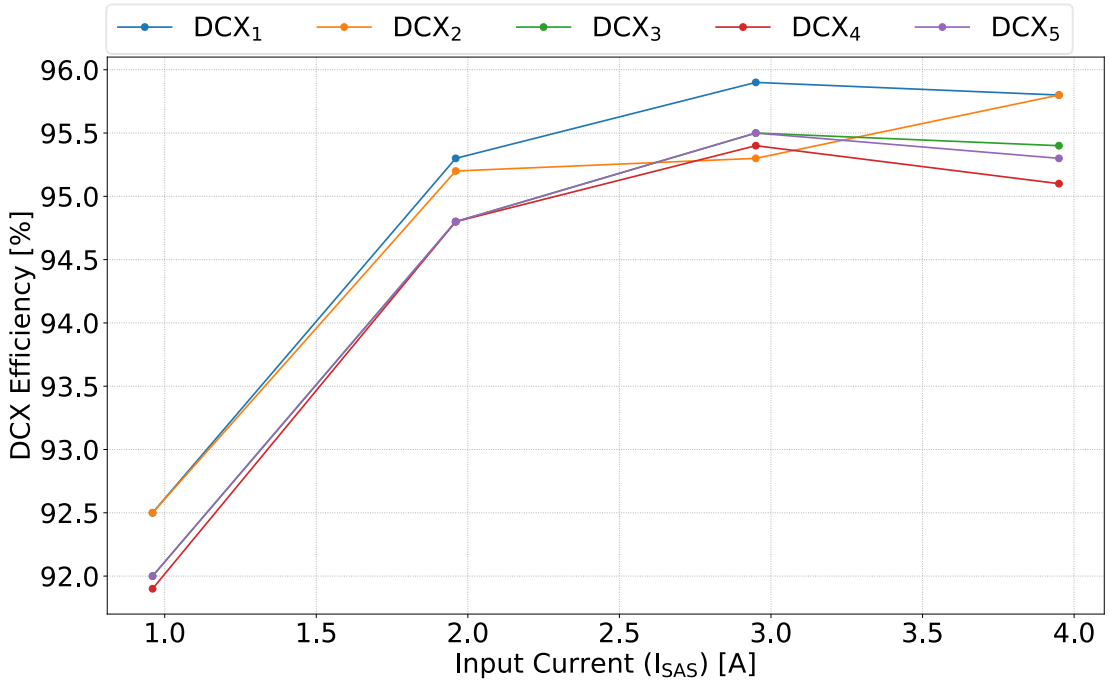

Figure 40. Measured efficiency of the five DCXs implemented at V_{SAS} = 100 V.

To observe the power losses distribution, the DCX_3 was continuously powered at 4 A for a period of 40 minutes at an ambient temperature of 25 ºC, while being monitored with a thermal camera. The transformer temperature, as well as the diodes-heatsinks and switching MOSFETs were measured, as shown in Figure 41. From these temperature readings, the power losses contributions for each component were estimated.

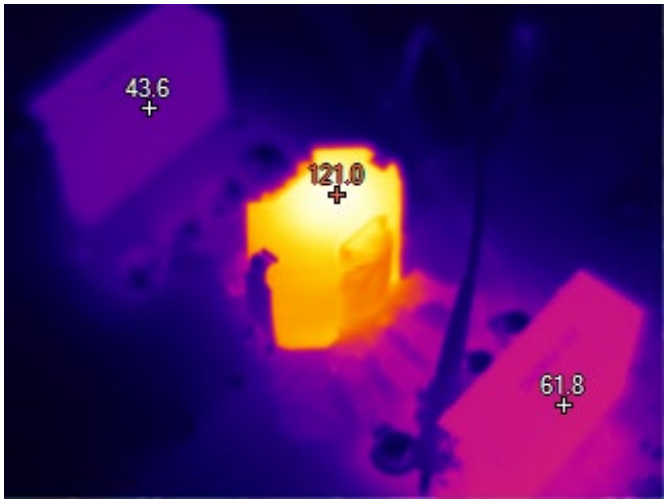

Figure 41. Thermal image of DCX_3 main hotspots. From left to right: Rectifier diode heatsinks (D_1, D_2), Transformer, MOSFETs (M_1, M_2). Temperature in ºC.

The heatsinks parameters [143], reveals that the MOSFETs heatsink experienced a 37 ºC temperature rise, which is indicative of 3,1 W dissipated power. Meanwhile the rectifier diode heatsinks exhibited a 19 ºC rise, indicative of a power dissipation of 1,7 W. Notably, the thermal dissipated power in both components is comparable to the theoretical values for the MOSFETs (48) and diodes (50). With respect to the transformer, it is observed that after 40 minutes, its temperature continued to rise and had not yet attained a stabilised state. The test was stopped after reaching 120 ºC to prevent any damage. After reviewing the information on the magnetic core [144], [145], it was concluded that transformer power losses required some reduction and two approaches were considered. Firstly, heat dissipation elements can be incorporated into the transformer. Secondly, hysteresis losses can be reduced. The latter can be achieved by using larger ferrite core, thus, decreasing f_{sw}, or reducing t_{on}. However, to avoid increasing the overall mass and volume of the converter, it has been decided to maintain f_{sw} while reducing t_{on}. This approach is further explored in section 4.4.2.

3.4.5 Driving and control loop implementation

Three main constraints have been considered for the driving circuit design. Firstly, fully analogue circuit design has been considered for simplicity and reliability purposes. Secondly, independent timing circuits are required for each DCX to cope with the variability of parameters that affect the resonant circuit. Thirdly, phase shifting is required to reduce high

frequency current ripple. Figure 42 shows the functional schematic of the implemented driving pulse generator.

The driving circuit comprises two distinct parts. Firstly, a common circuit, shared by all power cells, generates two sawtooth signals to define f_{sw}, and the voltage references for DCX interleaving. Secondly, the monostable section is independent for each power cell and generates the required t_{on} and interfaces with the MOSFET driver.

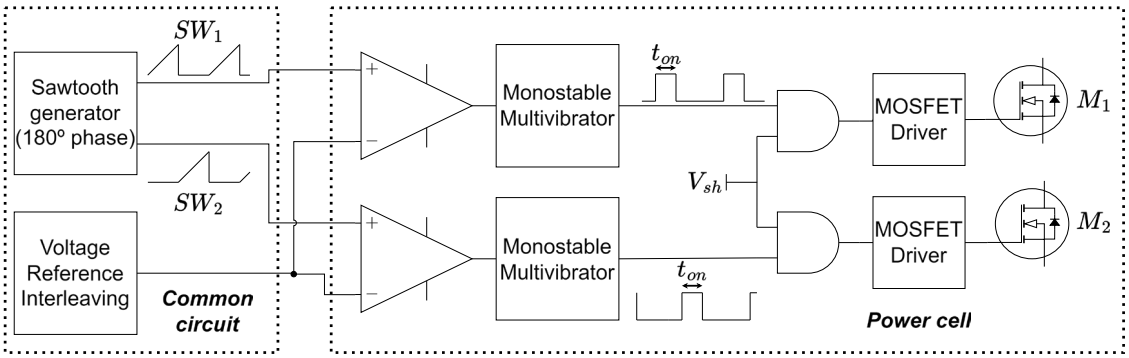

Figure 42. Functional schematic of analogue interleaved driving pulse generator.

The common circuit is implemented as shown in Figure 43. The multiphase silicon oscillator (LTC6902) generates two square signals that are 180° out of phase with each other. A current mirror is then used to charge a capacitor at a constant current. The corresponding phased-out square signal is used to discharge the capacitor, and eventually generates the sawtooth signal, SW. The frequency of the sawtooth signal determines the DCX switching frequency f_{sw}, and this can be easily adjusted by modifying the resistance $R_{f_{sw}}$. The voltage references used for interleaving purposes, THR_i, are generated from a simple resistive voltage divider, which voltage is stabilized by a Zener diode. Each THR_i is selected in such a way that optimal phase shift is achieved as the power cells are sequentially activated. Optimal phase shift is achieved in all cases, except when four power cells are connected, as represented in Figure 44.

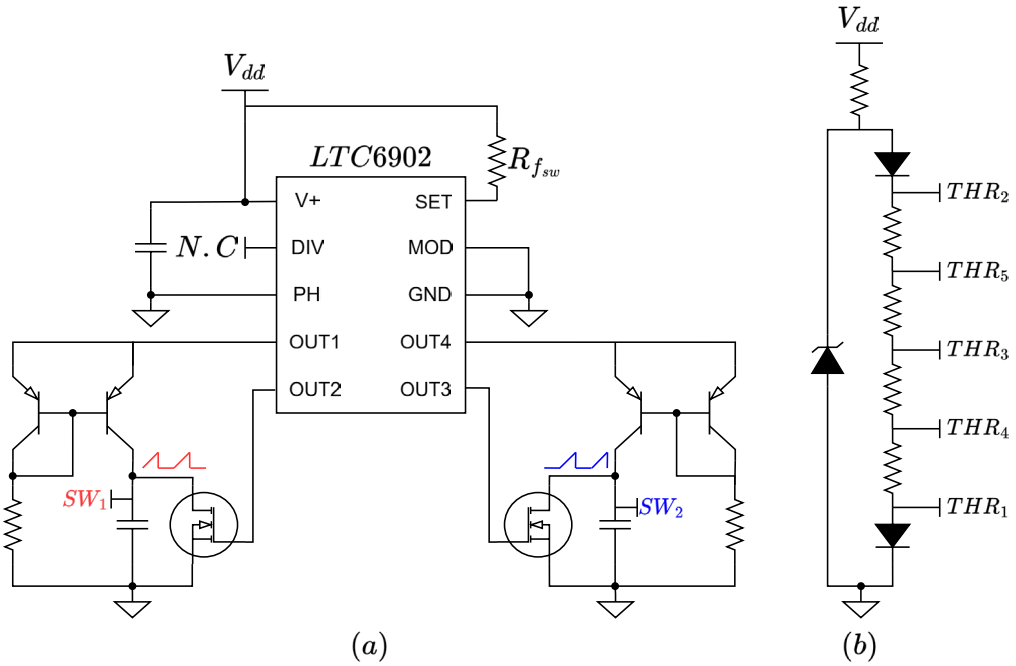

Figure 43. (a) Circuit schematic for phase sawtooth generator. (b) Circuit schematic for 5-phase interleaving voltage reference.

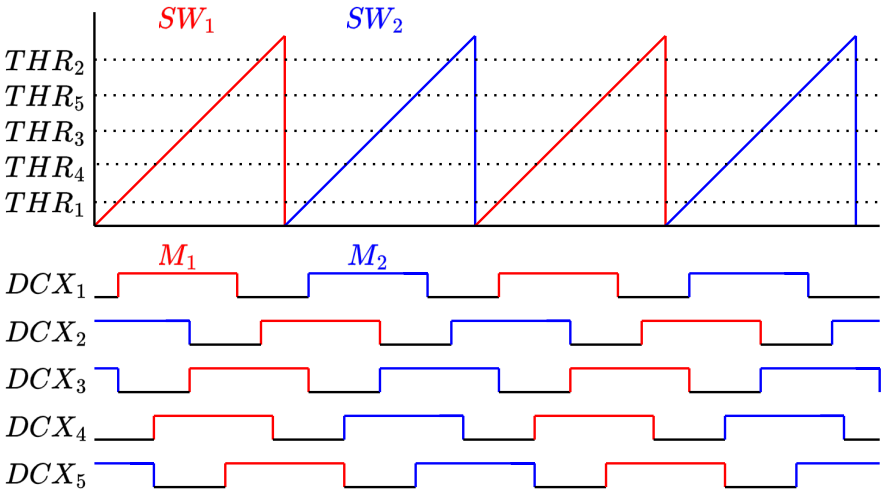

Figure 44. Top figure: Sawtooth signal and references voltages for interleaved switching. Bottom figure: Driving signals M_1 and M_2 for DCX_1-DCX_5.

Signals $SW1$ and $SW2$ are routed to each power cell and then compared to the corresponding voltage reference THR_i, as shown in Figure 45. The output signal triggers a monostable multivibrator (LTC6993), producing a pulse with a fixed duration, which can be adjusted by modifying $R_{t_{on}}$. These driving pulses, V_{dr}, are then used as control signals for the MOSFET driver (2EDN7524), which provides gate signals to M_1 and M_2. To prevent unnecessary switching noise, the MOSFET driver is deactivated, through V_{sh} signal, when

the SAS is shunted by the action of the S3R control loop. The gate resistance for turn-on and turn-off is selected to adjust the delay by equations (55), (56) and (57). The resulting driving signals are represented in Figure 46.

$$t_{d\,on} = R_g \cdot \frac{Q_{on}}{V_{th}} \tag{55}$$

$$t_{dr_{on}} = t_{on} + t_{d\,on} - t_{d\,off} - t_{d_m} \tag{56}$$

$$t_{dr\,off} = t_{gap} + t_{d_{off}} + t_{d_m} - t_{d\,on} \tag{57}$$

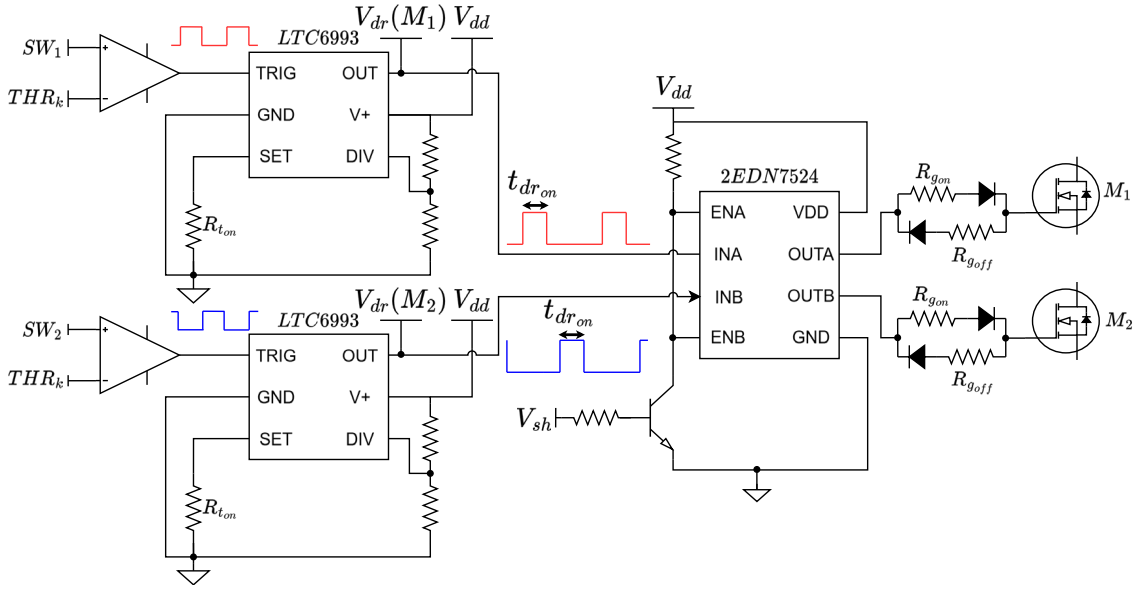

Figure 45. Circuit schematic for the push-pull DCX gate driving.

The MEA circuit is represented in Figure 47. The voltage sensing is accomplished through the implementation of a simple voltage divider made of HV resistors, R_k. To ensure galvanic isolation between the LV and HV sides, an isolated error amplifier (ADuM 3190), which has an equivalent space-grade version, has been employed. Considering the limited dynamic range exhibited by the ADuM, the proportional gain has been distributed across three stages. The integrator is placed on the first stage, before the isolator.

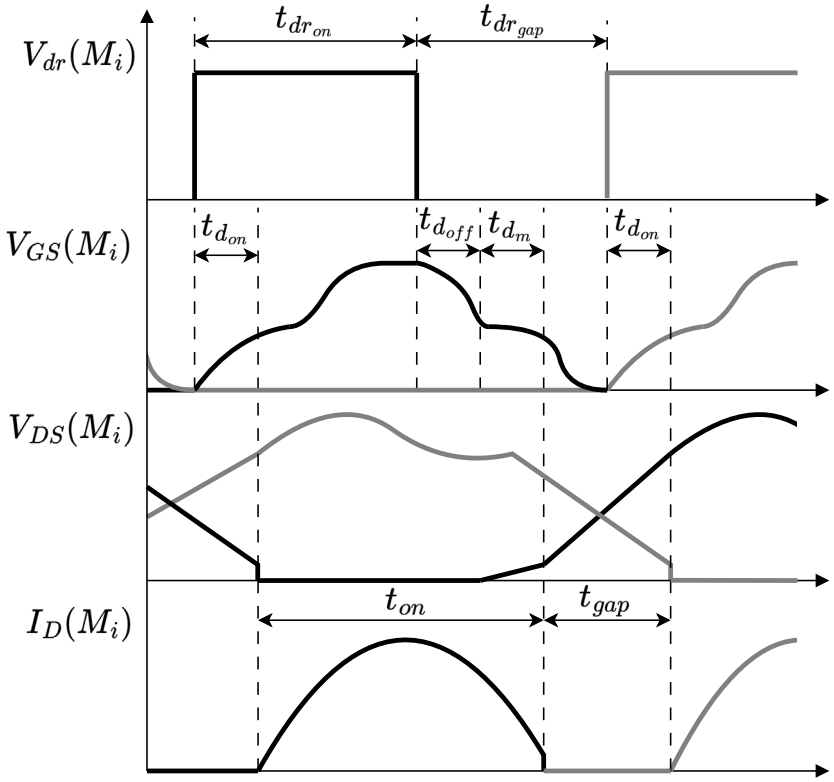

Figure 46. Driving signals and DCX waveforms

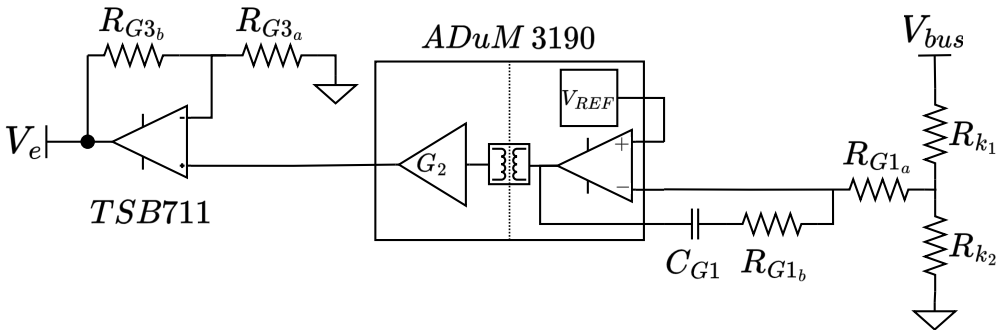

Figure 47. Circuit schematic for the isolated three-stage MEA

The sequential control of the S3DCX is managed using a hysteresis comparator which processes the voltage error, V_e, from the MEA. The high-frequency part of the V_e is filtered through a low-pass filter to eliminate interferences from the switching of the DCX. To prevent large current peaks during the discharge of C_{SAS}, a current limiter has been implemented. The current limitation value is determined by the activation of transistor Q, and the shunt resistor, R_{cl}, as defined in (58). The schematic of the S3R hysteresis comparator and current limiter is shown in Figure 48.

$$I_{LIM} = \frac{V_{BE(ON)Q}}{R_{cl}} = 14\ A \tag{58}$$

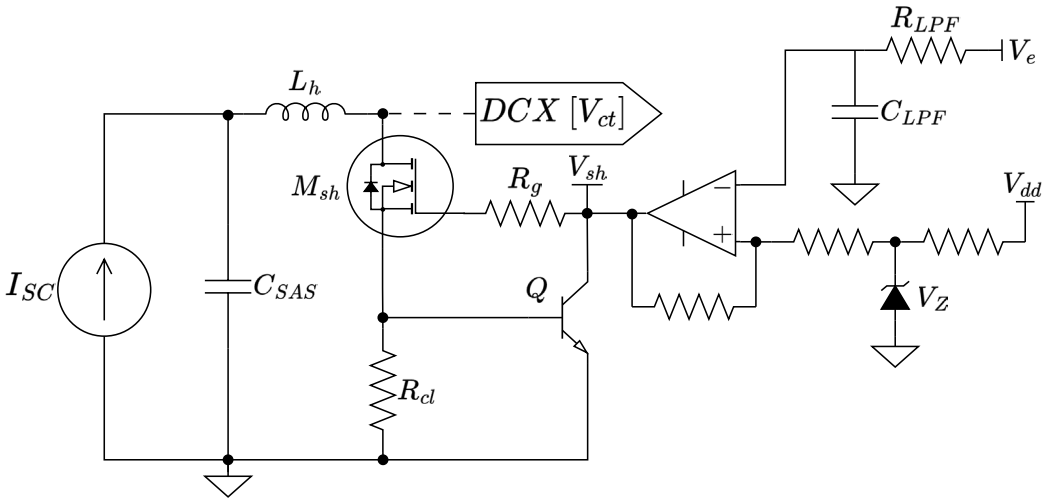

Figure 48. Circuit schematic for SAS hysteresis shunt control

An important part of the S3DCX is C_{BUS}, whose value significantly impacts the bus voltage ripple and transient response to load variations. C_{BUS} has been implemented using Metalized Polypropylene (MKP) film capacitors, as shown in Figure 49. These capacitors are characterised by their good self-healing properties, minimal losses and HV rating.

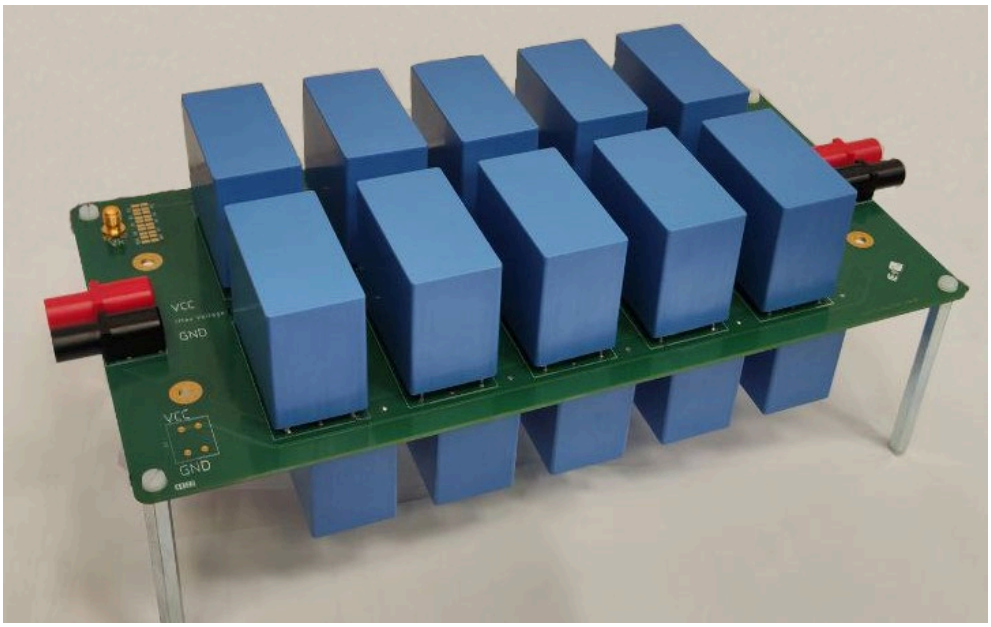

Figure 49. Bus capacitor – MKP film capacitor 390 µF, 1,3 kV.

The impedance of the implemented C_{BUS} has been measured using the Bode 100 vector network analyser [146] without including a DC bias, as show in Figure 50. The resonance frequency of C_{BUS} is 17 kHz. Up to 1 kHz the measured capacitance value is 390 µF and the Equivalent Series Resistance (ESR) is 3 mΩ.

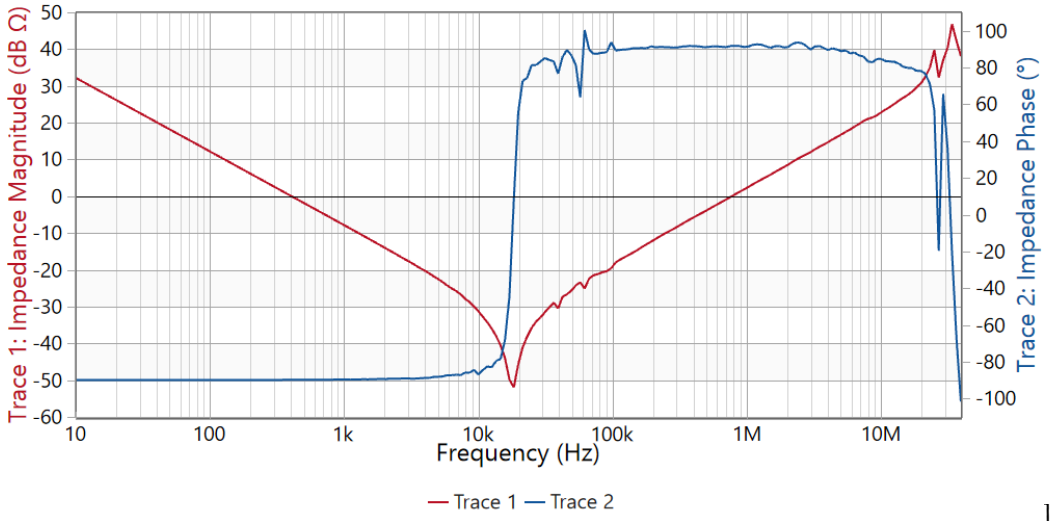

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Figure 50. Impedance gain (red) and phase (blue) of capacitor bus.

3.4.6 Multi-phase interleaving

Due to the resonant switching nature of DCX converters, the input and output currents are quasi-sinusoidal waveforms. If DCXs operate in phase, high peak current circulates in the bus, having a major impact on conducted emissions and power losses. A more effective approach to reducing RMS bus current is to interleave the DCXs. As the number of DCXs connected to the bus dynamically changes, the phase shift should be adapted depending on this.

The benefits of DCX interleaving have been evaluated using the S3DCX prototype with three power cells operating simultaneously at the regulation point of $V_{BUS} = 300\ V$ under a static power load of 950 W. In Figure 51, the D_1, currents of the synchronised DCXs and the bus current, which is the sum of the currents of D_1 and D_2 of all DCX before being filtered by C_{BUS}, are represented. The maximum value of I_{BUS} corresponds to three times the peak value of the DCX output current, reaching 9,5 A with a RMS value of 5,2 A. When interleaving is applied, as implemented in section 3.4.5, each DCX is equally phased-out, distributing the current pulses over a time period rather than concentrating them at a single

interval. In Figure 52 is represented the same experimental setup but including interleaving. With this implementation, both the peak current and RMS values are reduced to 6,3 A and 4,0 A, respectively.

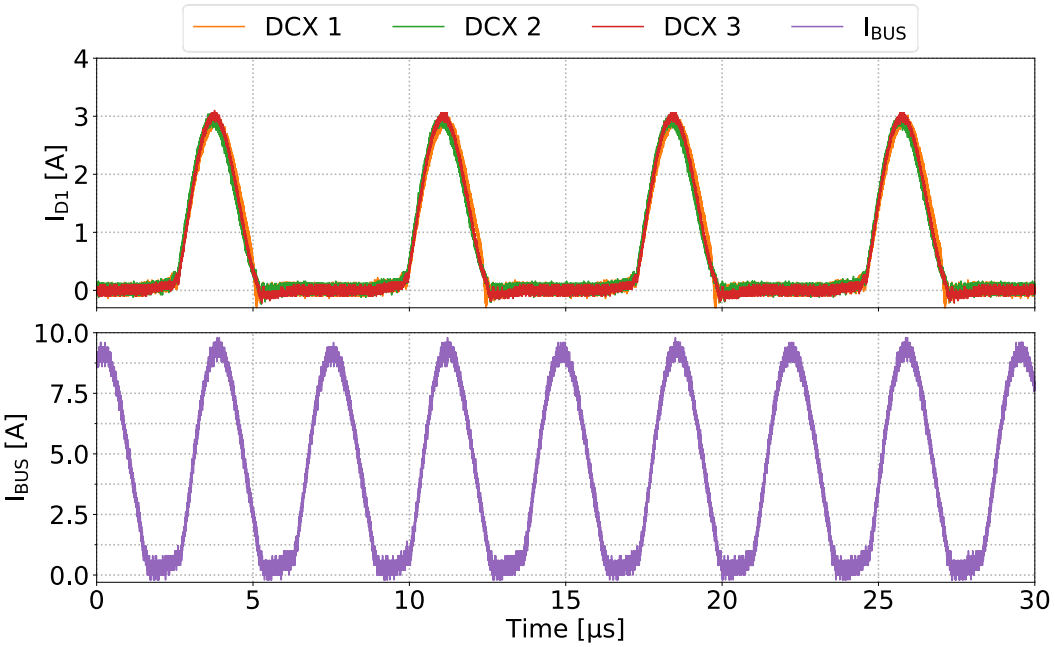

Figure 51. Output current without interleaved switching.
Top: Diode current D_1 DCX_1 *to* DCX_3. Bottom: Bus current (before C_{BUS}).

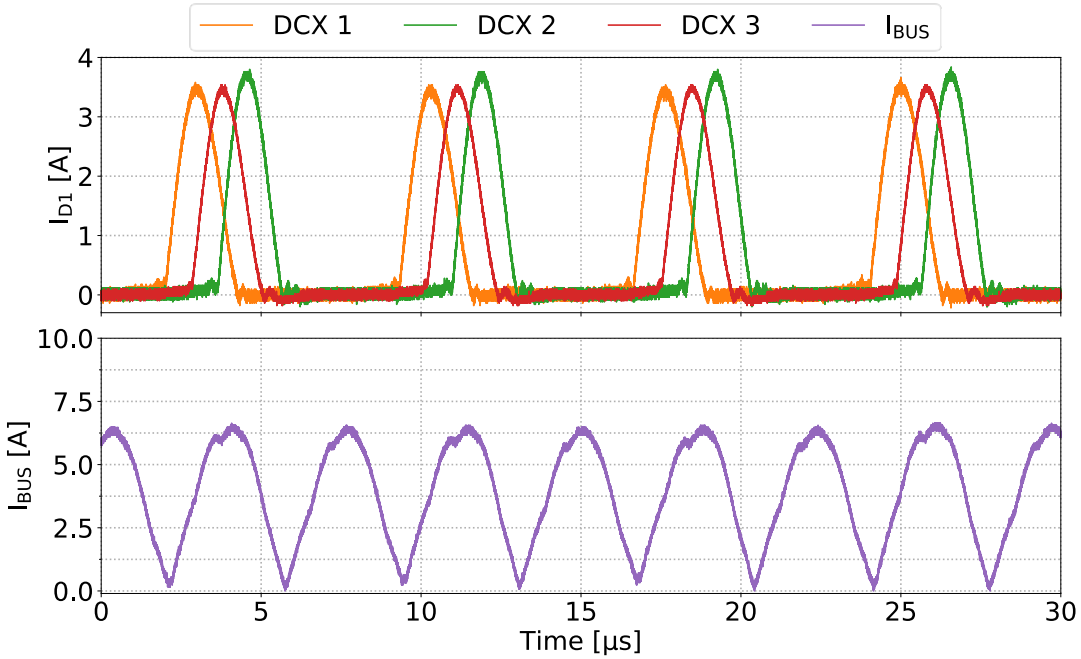

Figure 52. Output current with interleaved switching. Top: Diode current D_1 DCX_1 *to* DCX_3. Bottom: Bus current (before C_{BUS}).

3.5 Partial conclusions

This chapter presents, analyses, and extends the results of the article "*Sequential Switching Shunt Regulation Using DC Transformers for Solar Array Power Processing in High Voltage Satellites*" [132]. The main contribution of the article is the introduction of a novel concept for solar array regulation, called S3DCX, which provides a HV processing for a regulated distribution bus without requiring HV SAS. The concept has been meticulously modelled and experimentally validated with a prototype capable of processing 2 kW from a 100 V SAS to a 300 V distribution bus. Due to the modularity of the power cells, the outputs can be connected in series to increase the output voltage, allowing SAS at different voltages to be connected and converted simultaneously, and conditioned it to the desired distribution voltage.

Chapter 4

Article II: Enabling high-power conditioning and high-voltage bus integration using series-connected DC transformers in spacecrafts

In this chapter, the second article that forms part of the PhD thesis is presented, along with a comprehensive analysis of the results obtained.

Article II - [30]**: Enabling high-power conditioning and high-voltage bus integration using series-connected DC transformers in spacecrafts.** ***Aerospace*****, 11(8), 690,** Carlos Orts, Ausiàs Garrigós, David Marroquí, Antxon Arrizabalaga and Andreas Franke.

4.1 Summary

The following article proposes a photovoltaic power processor based on the S3DCX architecture, where power cells are serialized to achieve HV distribution buses for high power spacecraft. By extrapolating the requirements from ECSS-E-ST-20C [6], the study extends the bus voltage range from 300 V to 900 V to meet power demands up to 1,6 MW. Based on the implementation of the S3DCX presented in Chapter 3, a 100 V SAS is converted to 300 V at the output of the power cell. By serializing these outputs, bus voltages of 600 V and 900 V can be achieved, even under unbalanced SAS. The push-pull DCX topology imposes rectifier diodes with a voltage blocking capability of 800 V, for which SiC Schottky diodes present a potential solution. While these diodes outperform their silicon counterparts, they exhibit a high sensitivity to high-energy particle impacts, requiring a derating to prevent SEB. Current data shows that SiC Schottky diodes rated up to 1.700 V must operate below the required 800 V of the application, requiring a need of further development in radiation hardness [147]. Additionally, transformer isolation and power cell functionality are tested under partial pressure conditions and is validated for operation in high vacuum conditions.

The article is divided into six sections, which are distributed as follows:

- The methods to generate and condition HV and high power in spacecrafts are discussed in the **first section**.
- The requirements, market research and selection of power semiconductors compatible for the application are analysed in the **second section**.
- The working principle, modelling and simulations of the serialized power cells in the S3DCX to obtain a HV distribution bus is detailed in the **third section**.
- The serialized S3DCX prototype is validated, and the power cell and critical components are tested in vacuum conditions as detailed in the **fourth section**.
- The results obtained and the technological challenges are discussed in the **fifth section**.
- The article is concluded in the **sixth section**.

4.2 Article

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Article

Enabling High-Power Conditioning and High-Voltage Bus Integration Using Series-Connected DC Transformers in Spacecrafts

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Abstract: This article proposes a photovoltaic power processor for high-voltage and high-power distribution bus, between 300 V and 900 V, to be used in future space platforms like large space stations or lunar bases. Solar arrays with voltages higher than 100 V are not available for space application, being necessary to apply power conversion techniques. The idea behind this is to use series-connected zero-voltage and zero-current unregulated and isolated DC converters to achieve high bus voltage from the existing solar arrays. Bus regulation is then achieved through low-frequency hysteretic control. Topology description, semiconductor selection, design procedure, simulation and experimental validation, including tests in vacuum and partial pressures, are presented.

Keywords: satellite; high voltage; DCX; serialization; power semiconductor; Paschen law; vacuum environment

Citation: Orts, C.; Garrigós, A.; Marroquí, D.; Arrizabalaga, A.; Franke, A. Enabling High-Power Conditioning and High-Voltage Bus Integration Using Series-Connected DC Transformers in Spacecrafts. *Aerospace* **2024**, *11*, 690. https://doi.org/10.3390/aerospace11080690

Academic Editors: Xiaofeng Wu, Abdul-Halim Jallad, Yang Yang and Youngho Eun

Received: 18 July 2024
Revised: 17 August 2024
Accepted: 19 August 2024
Published: 21 August 2024

1. Introduction

To date, the International Space Station (ISS) is the space platform with the highest power generation capability, producing and distributing 105 kW [1]. The next space station, currently under development, is the Lunar Gateway, which is expected to handle 32 kW [2]. In both cases, power is generated by solar panels and a 120 V regulated bus voltage distribution is achieved through direct energy transfer (DET) power processors.

The current European space standard ECSS-E-ST-20C Rev.2 [3] defines the standard for regulated bus voltage at different power ranges up to 120 V. The standard states that 100 V or 120 V bus voltage is adequate in the range of 8 kW and 20 kW. However, for higher power levels, compliance with the standard becomes difficult in both static (large DC bus current) and dynamic (very low output impedance). Table 1 summarizes the different voltage and power ranges required to meet the strict output impedance mask dictated by [3].

Table 1. European space standard compliant voltage and power ranges for regulated bus [3]. In grey, extrapolated voltage and power ranges.

V_{bus} [V]	Max. P_{bus} [kW]	Max. I_{bus} [A]
28	1.5	54
50	5	100
100	20	200
120	28.8	240
300	180	600
600	720	1200
900	1620	1800

Larger space power systems are expected to arrive in the coming decades. Lunar bases and space stations would demand approximately 100–300 kW [4], and the initial attempts at space-based solar power will be in the MW range [5,6]. In all cases, these systems would be built in phases, resulting in the growth of the power requirement with each step taken, potentially surpassing initial design projections. Consequently, there is a substantial need for adaptable and scalable power generation and distribution systems capable of accommodating diverse requirements throughout each phase of deployment.

Different options have been considered for power systems in the order of hundreds of kW to few MW. One possibility is to use photovoltaic (PV) solar panels as the main power generator. The ISS has reached a total solar power production of 100 kW with an efficiency of 14.5% [1], and the new generation of European solar arrays for telecommunication satellites achieved a power production of 28.7 kW with an efficiency of 28.5% [7]. The main advantage of using solar arrays is the scalability and integration with the rest of the platform; however, for solar arrays operating above 150–200 V there are technical challenges to be solved [8].

Nuclear fission-based energy systems using Stirling engines have also been proposed for power ranges of tens of kW. However, this technology is not as mature as PV and scalability up to the hundred-kW range is not considered at this moment [9,10].

Regarding the electrical architecture, different solutions are explored to distribute high voltage (HV). In [11], a 1-kV bus is proposed for space solar power purposes. In [12,13], different power system architectures are studied for a lunar base. Both DC and AC microgrids might coexist, with typical voltages ranging from 120 V to 600 V. A common point in these examples is the significant distance between the PV generators and the end users. Therefore, the use of converters to integrate the PV generators into the distribution bus would be critical to provide regulation, galvanic isolation, and high voltage distribution. In this regard, the architecture described in [11] employs phase-shifted zero-voltage switching (ZVS) full-bridge converters in an Input Parallel Output Series (IPOS) configuration. A similar idea is proposed by the authors in [14], but the architecture is based on the current-fed zero-voltage zero-current switching (ZVZCS) direct current transformer (DCX) converter, described in [15]. Bus regulation is achieved using the Sequential Switching Shunt Regulator (S3R) technique, which consists of a sequential control of the DCX modules using a hysteretic controller [16]. Each power cell can be connected as an Input Independent Output Series (IIOS) configuration instead of IPOS for improved reliability. The main advantages of this approach are its simple switching control, regulation, and modularity. Moreover, the current-fed converter operates well with a solar array at the input. Furthermore, to keep the simplest transistor-driving approach, a push-pull and center-tapped full-wave rectifier structure is considered; see Figure 1. An explanation of the terms can be found in Table 4. On top of that, derating rules [17], limited availability of space-qualified parts [18], and high voltage isolation requirements [19] make the IIOS converter the most suitable approach. The architecture proposal is named by the authors as S3DCX.

The main research points of this article include a review of the state of the technology and availability of HV SiC Schottky diodes for space applications, with a focus on their voltage rating under the impact of high-energy particles. Additionally, this article covers the design and experimental validation of serialized DCX converters to achieve 600 V and 900 V distribution bus based on the S3DCX presented in [14]. The research also investigates the electric isolation of the DCX transformer and power cell in vacuum and partial pressure conditions.

Finally, this article is organized as follows. Section 2 analyses the requirements and derating needed to apply semiconductors for HV space applications. Section 3 details the serialization of the S3DCX to achieve 600 V and 900 V distribution bus. Section 4 presents the experimental validation of the output serialized S3DCX, the effects of the converter in vacuum, and partial pressure conditions. Section 5 discusses the experimental results. Section 6 concludes the article.

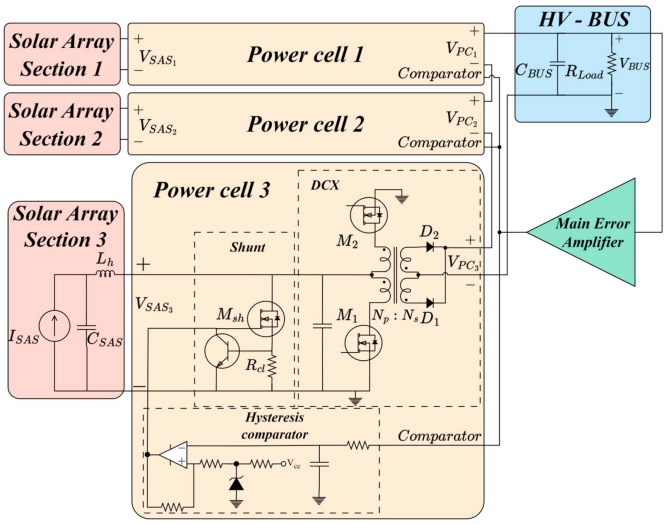

Figure 1. S3DCX: Three power cells in independent input-parallel output configuration.

2. Power Semiconductor Industry Market Research, Trends, and Selection

The harsh environment of space requires a selection of components that can work properly during the length of the mission. The European Space Standard ECSS-Q-ST-30-11C Rev.2 [17] is applied to avoid excess stress that could damage the components. In the S3DCX, MOSFETs and diodes are the most affected by the derating in the circuit. In general, power Field-Effect Transistors (FETs) must be 80% limited in V_{DS} and 75% in I_{DS} with respect to the maximum rating, and rectifier diodes must be 75% limited in I_F and V_R as well.

In a space environment, high-energy particles could impact the semiconductors, degrading their electrical properties or inducing a Single Event Breakdown (SEB). Depending on the transferred energy, defined by the Linear Energy Transfer (LET), the SEB will occur at different voltages. Therefore, it is crucial to ensure that the operating voltages remain within the safe operating area of the selected component.

Taking the proposal of this paper as a study case, 100 V is considered on the primary side of the power cell. So, the shunt FET (M_{sh}) and DCX FETs (M_1, M_2) must be rated, after derating, for a minimum of 125 V and 250 V, respectively. There are commercially available 250-V space-qualified MOSFETs that can sustain high LET at the rated voltage. In Table 2, a 250 V-45 A space-qualified MOSFET and a commercial equivalent have been selected for implementation in the prototype.

Table 2. 250 V-45 A Si MOSFETs in space qualified (top) and commercial equivalent (bottom) after derated ratings.

ID	Manufacturer	V_{DS} [V]	I_{DS} [A] T_c = 25 °C	R_{DSon} [mΩ] T_c = 25 °C	C_{OSS} [pF]
BUY25CS45B	Infineon	200	33.7	50	300
IXTQ42N25P	IXYS	200	31.5	84	300

Wide-Bandgap (WBG) FETs are considered for use in space applications due to their lower power losses, ability to operate at higher switching frequencies, and smaller size

compared to conventional Si FETs [20,21]. A demonstrator for an electrical propulsion power processing unit using Silicon Carbide (SiC) MOSFETs, operating at a maximum 500 V output voltage and 15 kW, has been tested, and the authors claim better performances compared to Si MOSFETs [22]. One challenge that makes it difficult to use WBG semiconductors is the significant derating required relative to their rated value to avoid SEB [23,24].

On the diodes side, for a 300-V output voltage, Schottky diodes are needed with a maximum repetitive peak reverse voltage (V_{RRM}) rating of 800 V after applying the derating and a minimum SEB threshold of 600 V. Nowadays, the maximum rating in Si Schottky diodes is 150 V [25], making them unsuitable for this application. An alternative is to use SiC Schottky diodes, rated up to 1.7 kV, with a lower recovery charge compared to the Si counterpart. One important aspect, as with FETs, is the large derating needed to avoid SEB. Different methods are being studied to improve it. In [26], simulations show that 1.2-kV SiC Schottky diodes are immune to SEB up to 800 V by using a lateral distribution of the semiconductor layers. In [27], charge-balanced regions between layers are introduced to improve the electric field distribution during a single event for 3.0-kV SiC Schottky diodes.

Figure 2 shows compiled different radiation test results for Si radiation-hardened (rad-hard) Schottky diodes [25]; commercial SiC Schottky diodes rated for 650 V [28], 1.2 kV [27–33], and 1.7 kV [28]; and laboratory SiC Schottky diodes rated for 3.0 kV [27]. SiC diodes rated for 1.2 kV and 1.7 kV must be derated to 200 V to avoid a SEB. It is shown that experimental 3.0-kV SiC diodes have a SEB threshold of 800 V, making them potential candidates for this kind of application.

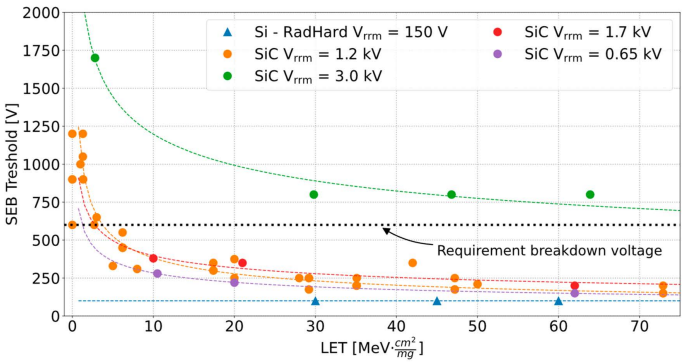

Figure 2. SEB threshold vs. LET. Commercial and experimental SiC diodes and space-qualified Si diodes [25,27–33].

From the analysis, it can be concluded that HV rad-hard SiC Schottky diodes are currently unavailable for space applications. Further technological development of SiC Schottky diodes is required to improve their reliability. Commercial SiC Schottky diodes could be used after applying a significant voltage derating [20], but additional studies regarding their suitability in a space environment are needed.

For the prototype development, and due to the lack of commercial SiC diodes of higher voltage, 1.2-kV SiC diodes have been selected, with the possibility of being replaced by 3.0-kV SiC diodes [27]. For the component selection, the Figure of Merit (FoM) (1) is utilized, which compares the forward voltage and the capacitive charge of the diodes. A lower FoM value indicates a better overall performance. The DCX operates under soft-switching conditions, so the capacitive charge of the diode will not significantly impact the losses but will affect the switching frequency. Table 3 summarizes a selection of commercially available SiC Schottky diodes rated for 1.2 kV-10 A and, for comparison purposes, a space-

qualified 150 V-20 A Si Schottky diode. Due to the lack of commercial devices and to ensure proper functioning in the worst-case scenario, the STPSC10H12 diode has been selected.

$$\text{FoM} = V_F \cdot Q_c \quad (1)$$

Table 3. Summary of commercial 1.2 kV-10 A SiC Schottky diodes. In grey, 150 V-20 A space-qualified Si Schottky diode for comparison.

ID	Manufacturer	Year	V_F [V]	Q_C [nC]	FoM (1)
STPSC10H12	STM	2016	1.25	47.5	59.4
C4D10120H	Wolfspeed	2019	1.30	44.0	57.2
IDM08G120C5	Infineon	2015	1.51	25.0	37.8
NDSH10120C-F155	Onsemi	2023	1.25	40.0	50.0
UJ3D1210K2	UnitedSiC	2020	1.25	44.0	55.0
VS-3C10ET12T-M3	Vishay	2024	1.25	47.5	59.4
GP3D010A120A	SemiQ	2019	1.30	47.5	61.8
STPS40A150CHR	STM	2020	0.82	13.2	10.66

3. Power Cell Serialization for High-Voltage Range

To regulate and increase the voltage from the solar panels to an HV distribution bus, the S3DCX topology [14] has been chosen. This topology allows each power cell to increase the input voltage of the solar arrays to an intermediate level and then serialize the outputs of each power cell to achieve the desired HV.

As shown in Figure 1, each power cell consists of three parts: a DCX converter implemented as a resonant ZVZCS push-pull converter, a MOSFET with a current limiter that shunts the Solar Array Section (SAS) to regulate the power cell voltage through controlled switching at a variable duty cycle, and a hysteresis comparator to control the regulation. Different power cells can be connected in parallel and controlled in a sequential manner for each hysteresis comparator by a main error amplifier (MEA).

The DCX can be analysed as an average model with a dependent voltage source at the input and a dependent current source at the output, as shown in Figure 3a. When the outputs of the DCXs are serialized, the bus voltage is the sum of the output voltage of each power cell, as defined in (2).

$$V_{BUS} = \sum_{i=1}^{N} V_{PC_i} = N \cdot \sum_{i=1}^{N} V_{SAS} \quad (2)$$

Following the averaged model, when current sources are connected in series at the output of each power cell, each SAS must deliver the same current, following the condition in (3), where I_{SAS} mean the current from the SAS, I_O the output current from the serialized power cells, and N the transformation ratio. If the I/V curves of the solar arrays are not identical, as shown in Figure 3b, the SAS with the lowest current will force the other SAS to operate on the right side of the curve, adjusting the voltage of each panel to reach an equilibrium point that satisfies (2), as demonstrated experimentally in [14]. A significant mismatch between SASs will have an impact on the overall power generation, as the operating point will be far from the maximum power point of the SAS, as shown in Figure 3c.

$$I_{SAS_1} = \cdots = I_{SAS_n} = \frac{I_{O_1}}{N} \quad (3)$$

A high-power space platform requires a large number of SASs due to the maximum power each SAS can generate, which is around 2 kW [7]. The power cells are connected in series to form a string, and these strings are connected in parallel to achieve the specified power output. Given the large number of SASs required, variations in temperature and irradiance can occur between different strings, reducing the power generated in the affected strings. Unbalanced solar arrays within the same string are less likely to occur since they

are physically close and, therefore, affected by similar operating conditions. At the system level, the impact of unbalanced strings can be minimised by adopting an architecture with multiple distribution buses, where each bus groups strings that operate under similar conditions. This approach could be beneficial in scalable high-power space platforms that expand over time, as it facilitates the deployment of solar groups and increases reliability compared to using a single distribution bus.

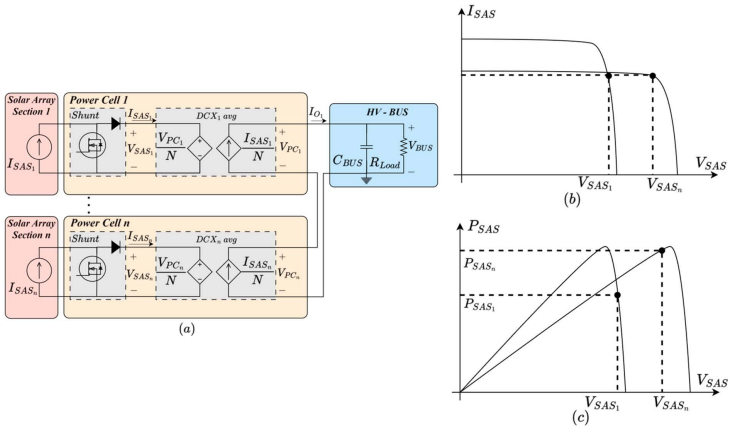

Figure 3. Serialized power cells. (**a**) Average model. (**b**) Generalized IV curve from SAS. (**c**) Generalized PV curve from SAS.

Computer simulation models in SPICE have been performed to validate the serialization of S3DCX. Each SAS is 100 V-4 A, and each power cell converts the output at 300 V. With two cells serialized, a 25% power step load simulation has been performed in Figure 4. The control loop has been designed to fulfil the requirements of the maximum voltage ripple defined in [3].

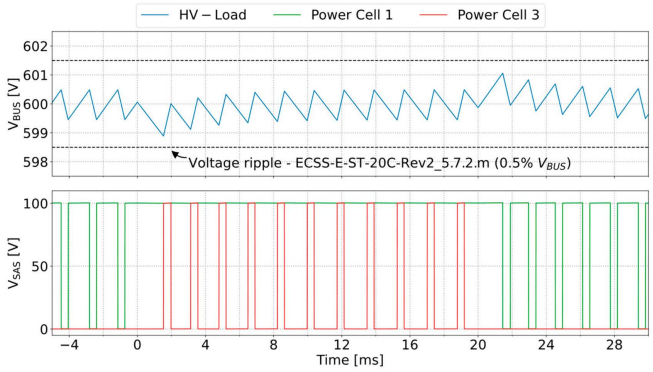

Figure 4. S3DCX with two power cells serialized. Top figure: distribution bus voltage. Bottom figure: Solar Array Section voltage.

In Figure 5, a second simulation with unbalanced SASs from 4 A to 2 A and three power cells connected in series to a constant power load has been performed. A constant

current of 2 A is supplied by each SAS but at different voltages. Due to the regulation of the voltage, the sum of the three outputs of the power cells remains at 900 V. The control loop has been designed to fulfil the requirements of [3].

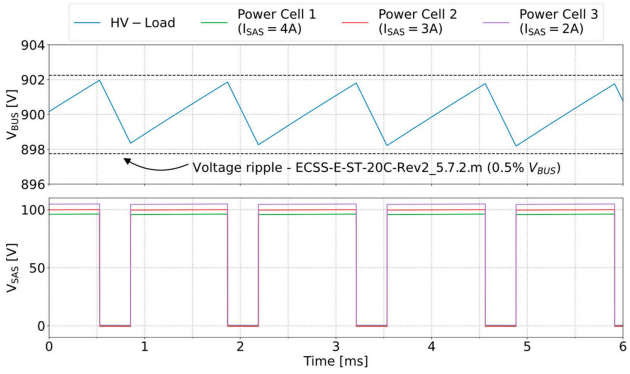

Figure 5. S3DCX with three power cells serialized. Top: distribution bus voltage. Bottom: Solar Array Section voltage.

4. Experimental Results

An S3DCX prototype has been implemented. Several tests have been carried out to validate the serialized power cells to achieve an HV distribution bus and study the behaviour and insulation of the converter in vacuum and partial pressure conditions.

4.1. Validation of a Serialized DCXs

Each power cell has been implemented for a power rating of 400 W, converting 100 V from the solar array to 300 V at the output of each power cell. By connecting the outputs in series, 600 V and 900 V distribution buses are achieved, as shown in Figure 6. Each power cell and SAS is designed and configured with the parameters defined in Table 4. The same prototype board is used for both 600 V and 900 V distribution bus, but only one can be active at a time. Swapping between configurations involves reconnecting the output series of the power cells and using the same signal from the hysteresis comparator for each string.

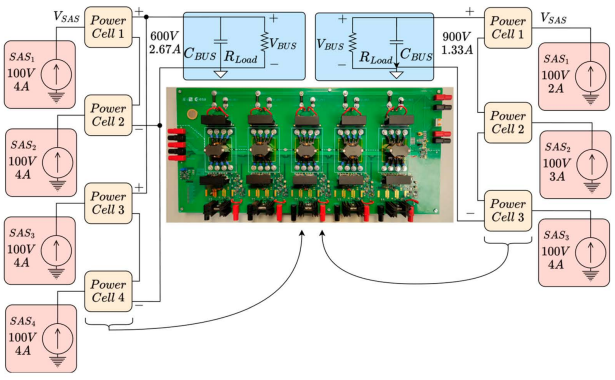

Figure 6. S3DCX experimental setup. **Left figure**: pair of two DCX in series (2s2p). **Right figure**: single string of three DCX in series (3s1p). **Center figure**: Prototype implementation of S3DCX.

Table 4. SAS and DCX design parameters.

Description	Value	Comment
Solar array section (SAS)—Agilent E4351B simulator		
V_{oc}	120 V	Open-circuit voltage
V_{mp}	110 V	Maximum power voltage
I_{sc}	4 A	Short-circuit current
I_{mp}	3.9 A	Maximum power current
C_{sas}	200 nF	Agilent E4351B
L_h	33 uH	Harness inductance
DCX transformer—push-pull		
Core	RM14	Material 3C95
$N = N_s/N_p$	15/5	V_{SAS} = 100 V; V_{PC} = 300 V
DCX and shunt circuit		
C_r	0.5 µF	CB182G0105J
M_1, M_2, M_{sh}	IXTQ42N25P	Si MOSFET (250 V, 42 A)
D_1, D_2	STPSC10H12	SiC diode (1.2 kV, 10 A)
DCX f_{sw}	135 kHz	D = 0.378
R_{cl}	50 mΩ	Max shunt current = 14 A

In a 2s2p configuration, as in Figure 6 (left), a power step load from 600 W to 1 kW has been performed for a 600 V bus. In Figure 7, during low power load, power cells 1 and 2 operate simultaneously to regulate the output voltage, while power cells 3 and 4 are off. After the step load, power cells 1 and 2 are on, but the power delivered is insufficient to the higher power demand and, therefore, power cells 3 and 4 deliver power at a given duty cycle to regulate the bus voltage. The voltage is stabilized after 6 ms. The steady voltage ripple is 1.6 V, which does not exceed the requirement of 0.5% of the bus voltage (3 V), as defined in the European Space standard in clause 5.7.2.m [3].

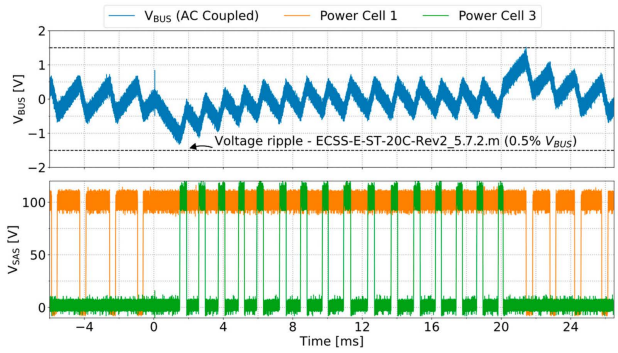

Figure 7. Experimental 2s2p S3DCX. **Top**: Distribution bus voltage (AC Coupled). **Bottom**: Solar Array Section voltage.

In a 3s1p configuration, as shown in Figure 6 (right), a steady power load of 800 W has been applied for a 900 V bus. Each solar array simulator is configured to operate within a current range of 2 A to 4 A, generating unbalanced inputs between the serialized power cells and forcing the current of the lower SAS. As a result, a difference in the solar array voltages can be observed at the input of the power cells, as shown in Figure 8. Despite the unbalanced SAS, the voltages of each SAS reach an equilibrium, ensuring that their

combined output equals 900 V of the regulated bus. The steady voltage ripple is measured at 3.5 V, which does not exceed the requirement of 0.5% of the bus voltage (4.5 V).

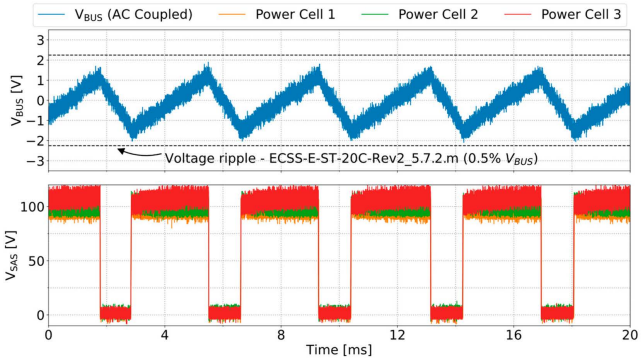

Figure 8. Experimental 3s1p S3DCX. **Top**: distribution bus voltage (AC mode). **Bottom**: Solar Array Section voltage.

4.2. Power Cell in Vacuum Conditions

In the European space standard, more than 200 V is considered HV and becomes an important design factor to avoid partial discharges, corona discharges, or arcing that could affect or damage the spacecraft [19]. To validate the S3DCX under space environment conditions, an isolation test of the DCX transformer and power cell was conducted in vacuum and partial pressure conditions, according to [19]. The tests were performed in the high-voltage laboratories of the European Space Research and Technology Centre (ESTEC) of the ESA. The experimental setup is shown in Figure 9.

Figure 9. High-voltage facilities with a vacuum chamber in ESTEC-ESA.

The DCX is implemented in a push-pull topology with a 300 V output, resulting in up to 600 V between the transformer windings. In ambient pressure, a non-destructive test was performed to check the dielectric withstanding voltage between the windings using a JP30A as equipment. For a duration of one minute for each pair of windings and in every combination, 600 V and 1.2 kV were supplied. In both cases, a leakage current under 1 µA was observed (isolation resistance > 10 GΩ), confirming that the DCX transformer can isolate voltages up to 1.2 kV.

During the Launch and Early Operation Phase (LEOP), the spacecraft is not completely depressurized, and partial pressures exist, creating the necessary conditions for corona discharge. The DCX transformer, being susceptible to such conditions, was tested in a vacuum chamber over a range of pressures from 10^3 mbar to 10^{-3} mbar with a constant

voltage of 600 VDC and limited to a maximum current of 2 mA. The experimental setup used is shown in Figure 10.

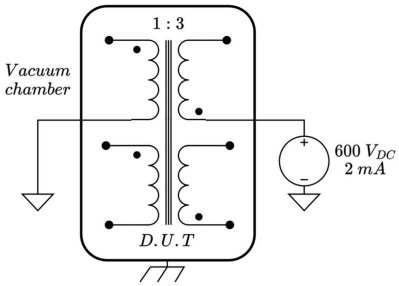

Figure 10. DCX transformer experimental setup for electrical isolation.

At the start of the test, the pressure inside the chamber is 10^3 mbar, the input voltage is measured at 600 V, and no current is flowing, indicating no current leakage or corona discharge. As the chamber begins to depressurize, due to the Paschen law, an electric arc occurs between the soldering joints of the primary and secondary winding within a pressure range between 0.8 mbar and 10 mbar, as observed in Figure 11. In this range, the voltage source is operating in constant current mode, meaning a current leakage. Outside of this pressure range, no current leakage or corona effect has been observed in the transformer, suggesting that electrical isolation within the core is maintained.

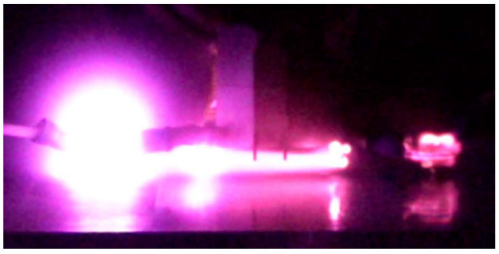

Figure 11. DCX transformer: Corona discharge at 1 mbar.

Analyzing the effects observed under partial pressure conditions shows that the transformer, for final implementation, must be modified to prevent HV points from coming into contact with the atmosphere. Some potential solutions include applying an electrically insulating coating layer on exposed parts or using planar transformers.

The next step is to verify that the power cell can operate under high vacuum conditions (10^{-4} mbar) using the experimental setup shown in Figure 12. The vacuum chamber is depressurized to the desired pressure, and then the circuit is powered on. During operation, a constant output at 300 V has been observed. On the power cell, the V_{DS} of the DCX MOSFET is measured, and it is verified that ZVZC conditions are still maintained, as shown in Figure 13. The waveforms observed are similar when operating under both ambient pressure and high vacuum conditions.

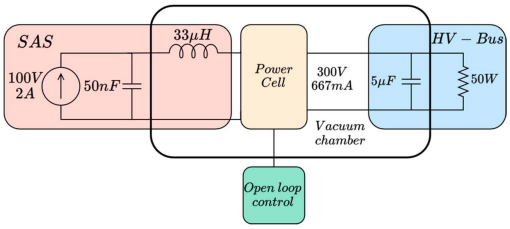

Figure 12. S3DCX experimental setup for validation and electrical isolation in vacuum and partial pressure conditions.

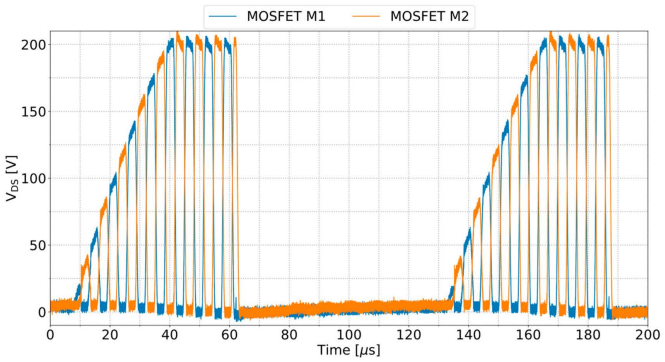

Figure 13. Drain source voltage (VDS) DCX MOSFETs at 10^{-4} mbar.

Using the same setup as in Figure 12, a decompression in the vacuum chamber was performed from 10^{3} mbar to 10^{-3} mbar with the converter powered on. During rectification, a reverse voltage of 600 V exists between the terminals of the diode. At 3 mbar, a corona discharge appeared between the pair of rectifier diodes until it stabilized in only one of them, as observed in Figure 14. At this pressure, the solar array simulator operates normally, with no faults detected on the primary side, thanks to the galvanic isolation. Power is transferred from the primary to the secondary; however, almost no current flows to the load due to the current discharge occurring between the diodes.

Figure 14. DCX power cell: Corona discharge in rectifier diode at 3 mbar.

Typical solutions to prevent a corona discharge between the terminals of the rectifier diodes include applying an electrically insulating coating layer to the electric components on the secondary side of the power cell or encapsulating via a potting the entire power cell. While potting ensures excellent electrical isolation, it comes with a significant trade-off in terms of increased weight and reduced thermal dissipation.

5. Results Discussion

Increasing the Technology Readiness Level (TRL) requires overcoming some technological challenges, yet it also presents advantages over alternative solutions. The S3DCX topology is based on two common techniques used in space applications, which simplifies reliability studies at the system level. However, the main obstacle is the lack of rad-hard SiC Schottky diodes for HV in space.

High-power space platforms that require HV distribution buses are still under development. Nowadays, a significant debate is whether to implement a single HV distribution bus or a dual bus architecture composed of a low-voltage bus to power most of the satellite systems and an HV bus dedicated to high-power payloads and electric propulsion. The dual-bus approach allows the HV bus to be deactivated during LEOP, a scenario characterized by partial pressure conditions, thus reducing the requirements for electrical isolation. However, this approach increases the overall complexity of the architecture. On the other hand, the single bus architecture is simpler in comparison, but increased efforts are needed to provide electric isolation on the HV component to prevent corona effects during LEOP operations.

The experimental implementation of the S3DCX employs 300 V power cell modules rated at 400 W, with serialization needed to achieve 600 V and 900 V distribution buses. The laboratory prototype requires a significant number of modules to handle the power processing for the HV distribution bus. Therefore, increasing power density is crucial to reduce the number of modules required and, in the process, eliminate the need to serialize power cells for HV buses. To achieve this, two methods can be explored, both requiring further development.

The first method involves increasing the voltage from the solar arrays to 300 V, removing the need to serialize for 900 V distribution bus at a transformation gain of 1:3. However, increasing the solar array voltages above 120 V introduces the risk of appearing electric arcs between the solar cells and slip rings, needing arc mitigation methods [8]. The second method, achieved by maintaining 100 V solar arrays, involves increasing the DCX transformation ratio to 1:6 and 1:9, with only one power cell required to achieve the 600 V and 900 V distribution bus. Both methods require an increase in the voltage rating and reliability for components such as MOSFETs, diodes, capacitors, and the electric isolation of the transformer.

6. Conclusion

This article presents a solution for generating, converting, and regulating the voltage from the solar array to the HV distribution bus for high-power space platforms by using an S3DCX topology. The serialized power cells achieve an HV distribution bus beyond 300 V, even with unbalanced solar panels. The DCX transformer and power cell have been studied in vacuum and partial-pressure environments. The power cell maintains ZVZC switching conditions at a constant voltage under a high vacuum. For a 300-V power cell, a 1.2-kV SiC Schottky diode was used in laboratory conditions. Further development is needed for higher voltage ratings and radiation hardened SiC Schottky diodes suitable for use in space environments.

Author Contributions: Conceptualization, A.G. and D.M.; methodology, C.O., A.G. and D.M.; software, C.O. and D.M.; validation, C.O.; formal analysis, C.O. and A.G.; investigation, C.O., A.G, D.M. and A.A.; resources, C.O., A.G., D.M., A.A. and A.F.; data curation, C.O. and D.M.; writing—original draft preparation, C.O.; writing—review and editing, C.O., A.G., D.M., A.A. and A.F.; visualization, C.O.; supervision, A.G. and A.F.; project administration, A.G.; funding acquisition, A.G. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the European Space Agency (Contract No.: 4000136441/21/NL/GLC/my).

Data Availability Statement: The datasets generated or analyzed during this study are available from the corresponding author upon reasonable request.

Acknowledgments: We acknowledge the support of Pablo Hernández and Oliver Korashy from the European Space Agency.

Conflicts of Interest: The authors declare no conflicts of interest.

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4.3 Motivation

The main motivation of this chapter is to extend the concept previously detailed in Chapter 3, S3DCX, and propose a photovoltaic power processor for HV, ranging from 600 V to 900 V, to adapt to very high-power distribution bus. A pivotal aspect of this study is the selection of power semiconductors capable of withstanding the space radiation environment, while addressing the challenges associated with HV operation.

The increasing demand for power in spacecraft, driven by advancements in electric propulsion systems [148], telecommunication satellites [38], space stations [37], and solar satellites [14], calls for higher voltage distribution systems. Currently, the ECSS-E-ST-20C [6] standard sets the maximum bus voltage at 120 V for power levels up to 28,8 kW. The current standard can be used to extrapolate bus voltage and maximum power for future high-power demanding applications, as listed in Table 11. For instance, a 1 MW electrical system, such as the SOLAIRS SBSP demonstrator [1], would require a 900 V bus voltage.

Table 11. Defined and extrapolated values (in grey) of voltage and power for regulated bus according to ECSS-E-ST-20C [6]. Extracted from [30].

V_{BUS} [V]	Max. P_{BUS} [kW]	Max. I_{BUS} [A]
28	1,5	54
50	5	100
100	20	200
120	28,8	240
300	**180**	**600**
600	**720**	**1.200**
900	**1.620**	**1.800**

In addition to other important considerations, HV and high-power spacecraft systems requires a careful analysis of power semiconductors. Silicon semiconductors have traditionally dominated, but the arrival of Wide-Bandgap (WBG) semiconductors offers significant improvements in efficiency, as well as mass and volume reduction. In terrestrial

applications, GaN HEMTs [149] and SiC MOSFETs [150] are the primary WBG options for controlled power devices, while SiC Schottky diode is commonly used as non-controlled WBG power device [151]. In the space environment, the most cumbersome aspect is the high susceptibility to SEB caused by high-energy particles, which is more pronounced in SiC than in GaN power devices [147], [152] requiring substantial voltage derating to mitigate potential SEB.

Partial pressure conditions that occur in certain phases in a spacecraft are another critical factor for HV systems. As defined in ECSS-E-HB-20-05A [25], voltages in excess of 200 V are categorised as HV. While the vacuum of space acts as an excellent electrical insulator, the depressurisation of the spacecraft during LEOP introduces partial pressures conditions. In such conditions, air can breakdown at a minimum voltage of 330 V, regardless of the distance between the exposed electrical terminal. This can lead to harmful phenomena such as corona discharges, partial discharges and arcing, which can interfere with or damage other spacecraft elements. To mitigate these risks, two main solutions are recommended, either the deactivation of HV systems during the LEOP phase or the incorporation of additional electrical insulation within HV components if the deactivation of HV systems is not feasible.

Taking these considerations into account, it seems clear that the analysis of output serialization in S3DCX converters is essential to establish HV distribution buses suitable for high power spacecraft systems. In addition, not only radiation robustness of power semiconductors, but also efficiency is of paramount importance to evaluate. Finally, testing in partial pressure conditions is also of interest in order to identify the critical components susceptible to HV effects, like corona discharges or arcing, and to define methods to mitigate the risks.

4.4 Article analysis

The modularity of the S3DCX allows HV bus regulation beyond 300 V through the connection of the power cells outputs in series. For the effective operation of S3DCX with output series connection, all power cells within a string must share the same hysteresis reference and operate with synchronized switching signals. In an output-serialized configuration, the output current is the lowest current of all SAS, and consequently, the voltage of each SAS will move freely to the point that current is the same, as illustrated in

Figure 53. This leads to two key conclusions, first, photovoltaic power extraction may be compromised if the current to voltage characteristics differ significantly; and second, while voltage equalisation cannot be guaranteed between power cells, the voltage feedback loop ensures that the sum of these different voltages equals to the required bus voltage.

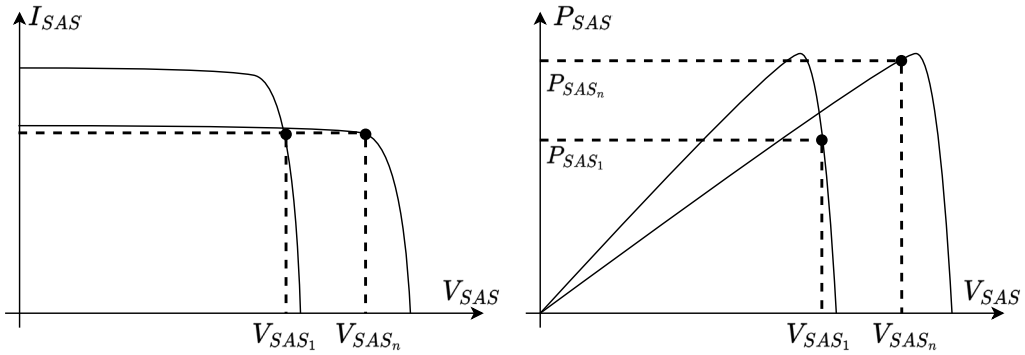

Figure 53. Unbalanced SAS in serialized power cells.
Left: Generalized I-V curve from SAS.
Right: Generalized P-V curve from SAS. Extracted from [30].

A series of experiments were carried out using the prototype detailed in Chapter 3 to study and validate the use of output serialised power cells, and the schematics can be found in Annex I. Distribution buses of 600 V and 900 V were derived from 300 V power cells and 100 V SAS. In addition, the SAS were configured with different levels of I_{SC}, between 2 A and 4 A, to examine the response and operation of the system under unbalanced conditions. The experimental setup used in both configurations is shown in Figure 54 and described in Annex II.

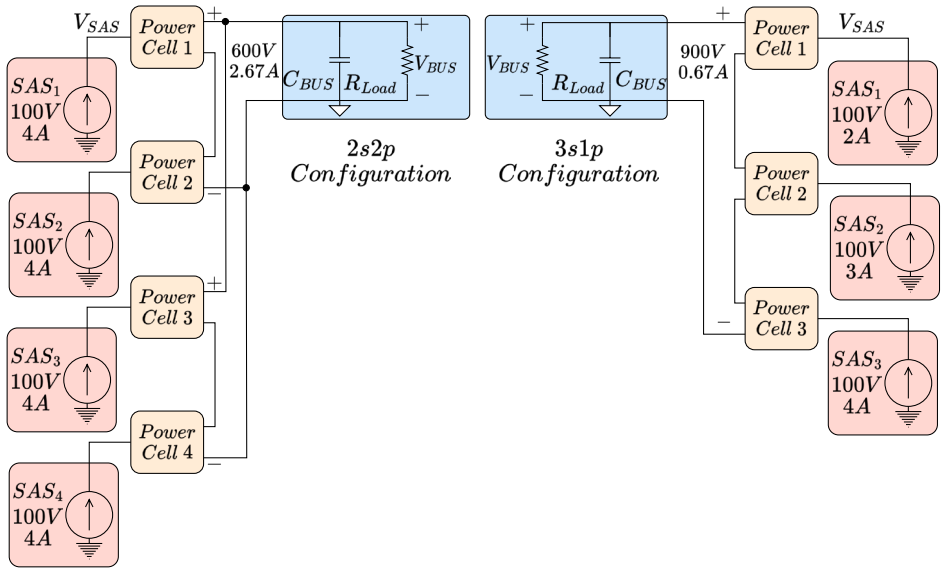

Figure 54. S3DCX experimental setup with output-series connection.
Left: Configuration: 2s2p for 600 V bus. Right: Configuration: 3s1p for 900 V bus.

Paschen's law states that the breakdown voltage of air is 330 V under specific pressure-distance conditions. In this design, the power cell generates 300 V at its output, which is below the breakdown voltage. However, due to the push-pull structure, more than 600 V appears in the transformer and the rectifier diodes, ensuring corona discharge and electric arc issues in partial pressure conditions. As a preliminary study, a campaign of tests was conducted to evaluate the internal insulation under ambient, partial and high vacuum pressure conditions. The experimental prototype used for this purpose is shown in Figure 55.

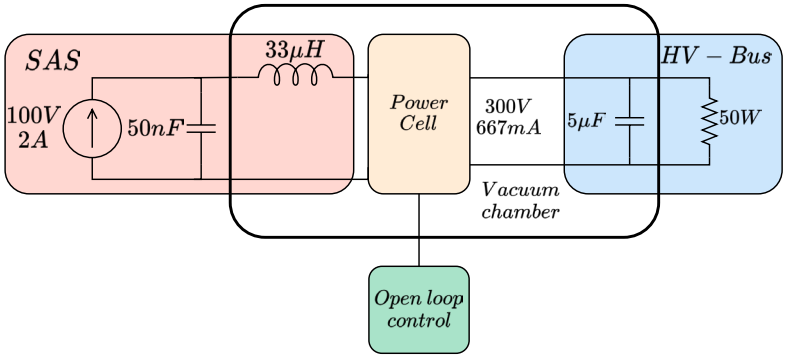

Figure 55. Single power cell experimental setup for validation and electrical isolation in vacuum and partial pressure conditions. Extracted from [30].

4.4.1 State of HV semiconductors for space applications

The space environment is characterised by the constant exposure of energised particles, which degrade the performance of electronic components over time as function of the Total Ionising Dose (TID). Under certain conditions, high-energy particles can cause SEE. Among the different possible options, SEB is considered one of the most critical of these effects. SEE can arise in different component types, but power semiconductors, given their function nature, are particularly critical elements. The standard ECSS-Q-ST-30-11C [33] defines the derating requirements for electronic components to ensure a reliable operation throughout their expected lifespan, given the harsh conditions of space. Key components affected include the switching FETs (M_1, M_2 and M_{sh}) and the rectifier diodes (D_1 and D_2) in the power cell, which must withstand voltages in excess of 100 V, narrowing the selection of suitable options.

As outlined in section 3.4.4, the characteristics of switching FETs have a significant impact on the overall efficiency of the DCX. Conduction losses are mostly influenced by r_{on}, while the required t_{gap}, necessary for discharging the parasitic capacitances, affects the I_{RMS} and the overall sizing of the DCX. Therefore, r_{on} and C_{oss} are the two main parameters of the FETs to be evaluated based on the figure of merit presented in [153] which is calculated using equation (59).

$$NHFFOM = \frac{1}{r_{on} C_{oss}} \tag{59}$$

The required BV_{DSS} for the switching FETs, considering an 80 % of voltage derating specified in the standard [33], is 250 V. On the other hand, assuming that I_{RMS} is approximately 1,5 times greater than I_{SAS} and a 75 % current derating defined in the standard [33], the I_D required is 8 A. A total of 58 FETs, including silicon and WBG transistors, that meet these conditions, were considered as candidates, as summarised in Table 12. A complete list of the selected components is detailed in Annex IV.

Figure 56 presents the New High Frequency Figure of Merit (NHFFOM) of the FETs evaluated against the breakdown voltage. The minimum, maximum and median value for each semiconductor at a given BV_{DSS} are highlighted, and some conclusions can be drawn from this analysis. Firstly, radiation hardened Si MOSFETs perform poorly compared to WBG semiconductors. Secondly, in the 600 V to 650 V range, GaN is slightly better than SiC. Thirdly, in the 1.200 V voltage range, SiC shows a large dispersion but a similar median value to that of 650V devices. Finally, there is a special case in the middle, the 750 V SiC cascode, which has a very competitive NHFFOM, better than any other, making it promising option for use as a switching FET.

Table 12. General description of the types of FETs considered for DCX.

Semiconductor	BV_{DSS} [V]	No. References
Si RadHard	250	2
Si RadHard	650	1
SiC	650	19
SiC	1.200	9
GaN	600	5
GaN	650	9
GaN RadHard	200	2
GaN Cascode	650	8
SiC Cascode	750	2
SiC Cascode	1200	1
Total number of references		58

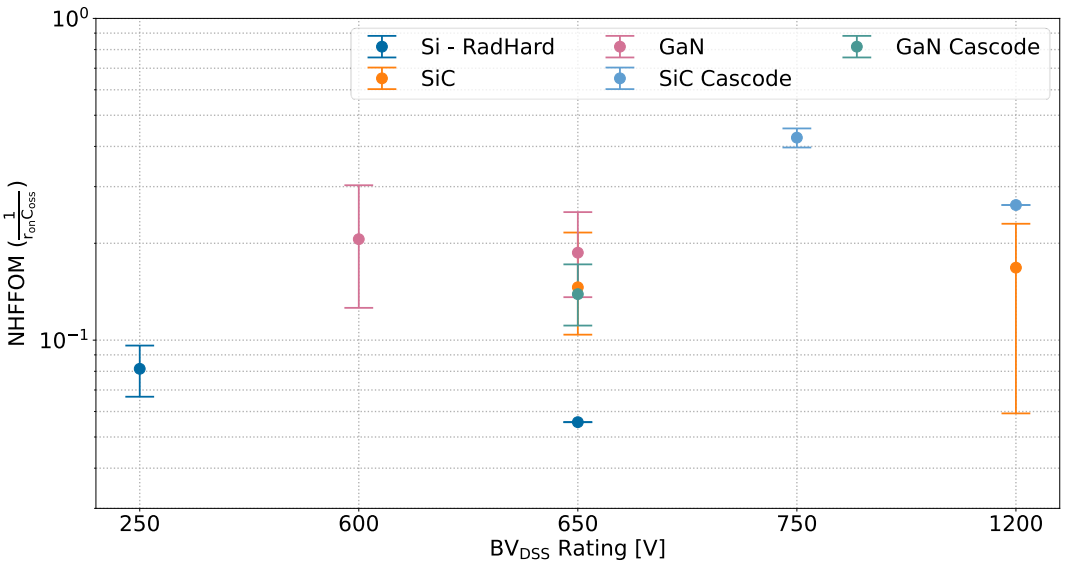

Figure 56. FET evaluation: NHFFOM vs BV_{DSS}

One of the critical issues for adopting WBG power devices is their susceptibility to SEB. Different SEE radiation tests for FETs with a minimum BV_{DSS} of 250 V have been analysed, please refer to Table 13.

Table 13. Literature review of FETs tested against SEB.

Component	Manufacturer	Semiconductor	$BV_{DSS}\ [V]$	$I_{DS}\ [A]$	Ref.
BUY25CS54A	Infineon	Si RadHard	250	34	[154], [155]
BUY65CS08J	Infineon	Si RadHard	650	5	[156], [157]
C2M0080120D	Wolfspeed	SiC	1.200	24	[158]
SCT20N120	STM	SiC	1.200	16	[159]
PGA26E07BA	Panasonic	GaN	600	31	[160]
PGA26E19BA	Panasonic	GaN	600	15	[161], [162]
GS66508P	GaN Systems	GaN	650	25	[160]

In Figure 57 is represented the minimum voltage at which SEB occurs for the analysed FETs. The data have been segmented into different groups based on semiconductor technology and BV_{DSS}. For the sake of clarity, Linear Energy Transfer (LET) values of 0,01 $MeV\frac{cm^2}{mg}$ indicate tests performed using protons. The main conclusion obtained from this analysis is that the GaN devices perform better than SiC MOSFETs even having lower BV_{DSS}. The worst case for the SiC MOSFETs is 200 V for a LET of 30 $MeV\frac{cm^2}{mg}$, i. e. the 16,7 % of its BV_{DSS}, falling into the critical zone to work with 100 V solar arrays. There are not public SEE tests for the SiC cascode, which has the best NHFFOM.

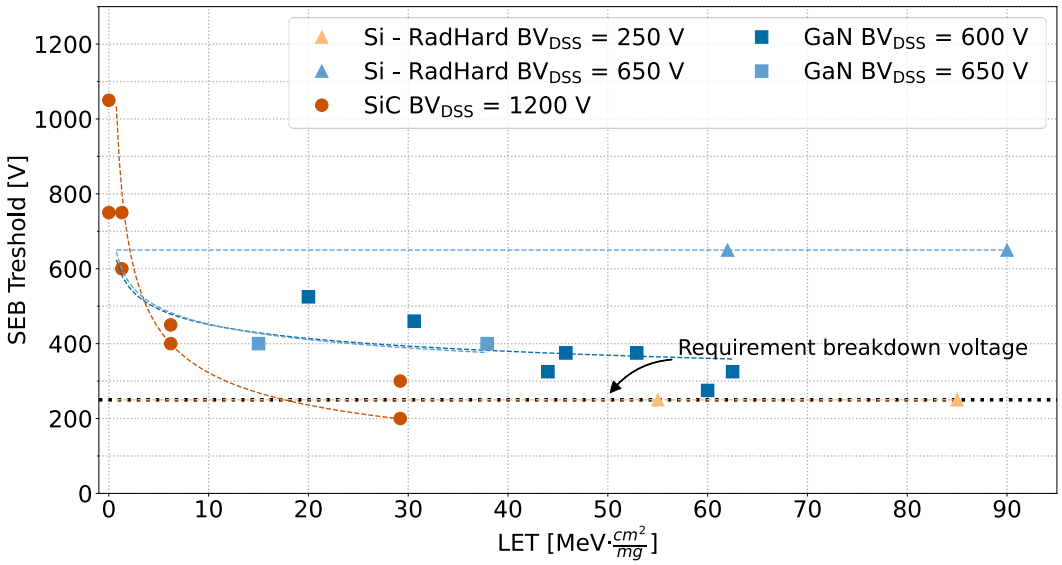

Figure 57. SEB threshold vs LET.
Commercial SiC and GaN FETs and radiation hardened Si and GaN FETs.

The figure of merit used for evaluating the rectifier diodes considers the diode forward voltage, V_F, and the total capacitive charge, Q_C, (60), based on the figure of merit presented in [163]. Both parameters affect the converter efficiency. In particular, Q_C impacts on t_{gap} and eventually on the I_{RMS}.

$$FoM = V_F \cdot Q_C \tag{60}$$

With a 1:3 transformation ratio, the rectifier diode will require 750 V of V_{RRM} and 2,67 A of I_F. To achieve low t_{gap}, low Q_C diodes are preferred, reducing the selection to SiC Schottky diodes. A total of 19 diodes, were evaluated as summarized in Table 14. Additionally, radiation hardened 400 V Si diodes were included for comparison. A complete list of the considered components is provided in Annex IV.

Table 14. General description of analysed SiC diodes.

Semiconductor	V_{RRM} [V]	No. References
Si RadHard	400	1
SiC	1200	16
SiC	1700	2
Total number of references		19

As illustrated in Figure 58, the FoM of the diodes evaluated against the breakdown voltage is presented. The minimum, maximum and median value for each semiconductor at a given V_{RRM} are highlighted. It is clear that 1.200 V is the best performing of the three.

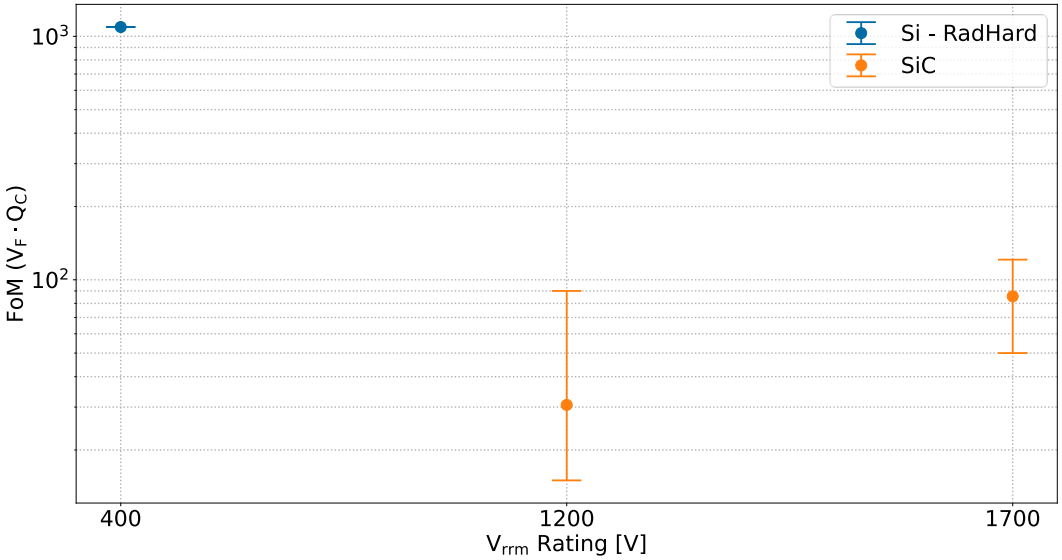

Figure 58. Distribution of diodes candidates regarding their FoM respect the rated V_{RRM}.

Various SEE radiation tests have been compiled for SiC diodes with a minimum V_{RRM} of 750 V and relevant information have been summarized in Table 15. Radiation hardened Si diodes has been included as a baseline.

In Figure 59 is represented the minimum voltage at which SEB occurs for the analysed diodes. The data have been segmented into different groups based on semiconductor technology and V_{RRM}. For the sake of clarity, LET values of 0,01 $MeV\frac{cm^2}{mg}$ indicate tests performed using protons. It should be noted that, this figure is an updated version of the one originally presented in [30].

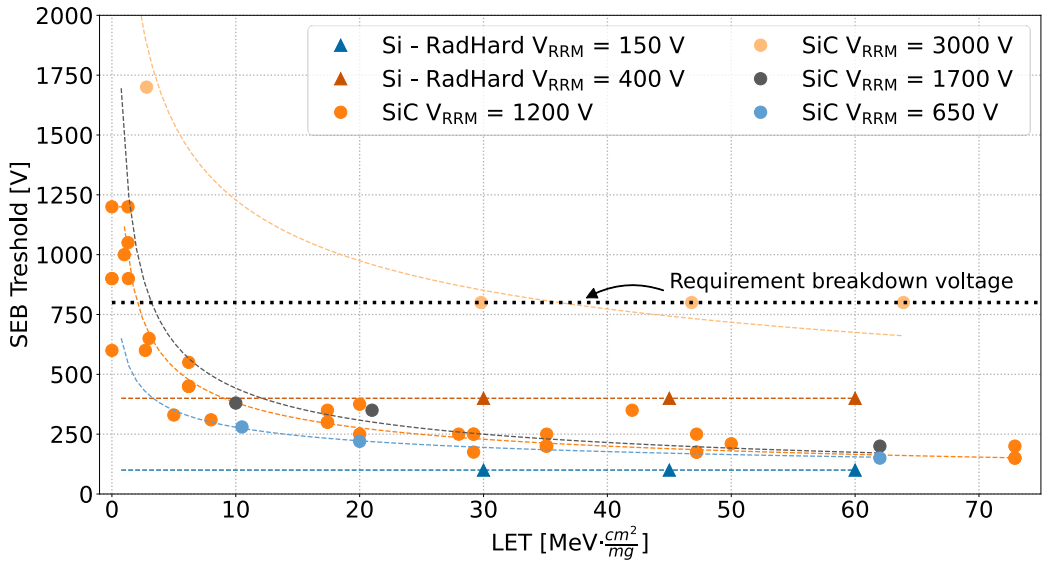

Figure 59. SEB threshold vs LET. Commercial SiC and radiation hardened Si diodes.

Table 15. Literature review of diodes tested against SEB.

Component	Manufacturer	Semiconductor	V_{RRM} $[V]$	I_F $[A]$	Ref.
STPS40A150CHR	STM	RadHard Si	150	17	[164]
STTH60400HR	STM	RadHard Si	400	31	[165]
STPSC10H065	STM	SiC	650	10	[166]
IDW10G120C5B	Infineon	SiC	1.200	8	[167]
C4D40120D	CREE	SiC	1.200	27	[168]
SML020DH12	Semelab	SiC	1.200	10	[169]
STPSC6H12	STM	SiC	1.200	10	[170]
GB20SLT12-247	GeneSiC	SiC	1.200	32	[171]
C4D020120A	Wolfspeed	SiC	1.200	5	[166]
CPW5-1700-Z050B	Wolfspeed	SiC	1.700	10	[166]
Charge-Balanced JBS	General Electric Research	SiC	3.000	-	[172]

Data analysis indicates that commercial 650 V and 1.200 V SiC Schottky diodes exhibit a SEB susceptibility below 400 V even at low LET levels, being very similar to SiC MOSFETs, and only the 3.000 V SiC diode [172] would meet the required breakdown voltage. The implementation of a full-bridge diode rectifier would alleviate this problem by reducing the required voltage to 375 V, but even then, commercial SiC Schottky diodes would not meet the voltage requirements in most cases. This is identified as critical point for the adoption of the technology. Fortunately, recent studies have demonstrated better tolerance to SEB with other approaches, such as lateral SiC Schottky diodes [173], [174].

4.4.2 Increasing power capabilities with WBG semiconductors

One key advantage of the proposed DCX converter is that the input current, I_{SAS}, can be increased without affecting its resonant performance, in other words, t_{on} and t_{gap} do not depend on input current, as expressed in (25) and (32). Furthermore, since the output voltage is regulated, the input voltage is tightly controlled and the risk of saturating the transformer magnetic core is avoided, since this depends on two constant parameters, V_{SAS} and t_{on}, as defined in (37). However, an increase of I_{SAS} has a direct effect on the RMS current flowing through the DCX, I_{rms}, and ultimately on the conduction power losses, as well as reducing the ideal ZVS condition due to the increase in v_{on}, as expressed in (35).

In order to evaluate the performance of the DCX converter under high solar array current conditions, three solar array simulators were connected in parallel to a power cell whose parameters are summarized in Table 6 and Table 10, as shown in Figure 60. In these tests, taking into consideration the full schematic of the S3DCX in Figure 23, the input inductance was removed and the remaining inductance, $L_h = 3\ \mu H$, is the parasitic inductance of the cable connecting the solar array simulators to the power cell, and no additional changes were made from the original 4 A design.

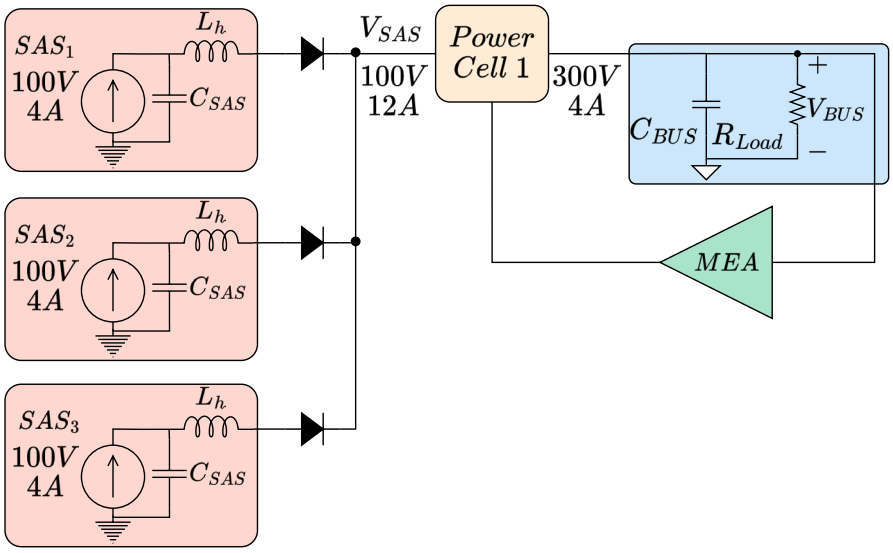

Figure 60. S3DCX experimental setup with a single power cell and multiple SAS in parallel.

Different tests were carried out by varying $\sum I_{SAS}$ from 4 A to 12 A at 300 V output. Figure 61 displays the M_1 voltage and D_1 current within these limits. At maximum input power, the ZVS degrades as the turn-off voltage, v_{on}, increases from 10,5 V to 38,4 V, but there is no significant effect on MOSFET switching losses. Another result of higher input current is the voltage ripple of C_r, which rises from 47 V to 64 V, resulting in an increase of V_{DSpeak} from 232 V to 246 V. A theoretical analysis of the power losses at different I_{SAS} values reveals a significant drop in efficiency at higher currents, as detailed in Table 16. This decline is mainly due to conduction losses, P_{cond} in the switching MOSFETs M_1 and M_2, P_d in the rectifier diodes D_1 and D_2, and P_{Wn} in the transformer windings. The resonant capacitor losses, P_{Cr}, are also affected but to a lesser extent than the other losses. Finally, the core losses, P_{hyst}, remain unchanged, as V_{SAS} and t_{on} are unaffected.

As shown in Table 16, the most limiting factor in increasing the power of solar arrays is the conduction losses of the primary switches. Different types of power semiconductors have been identified and selected to improve the efficiency. A comparison of the main parameters of different candidate WBG transistors is shown in Table 17.

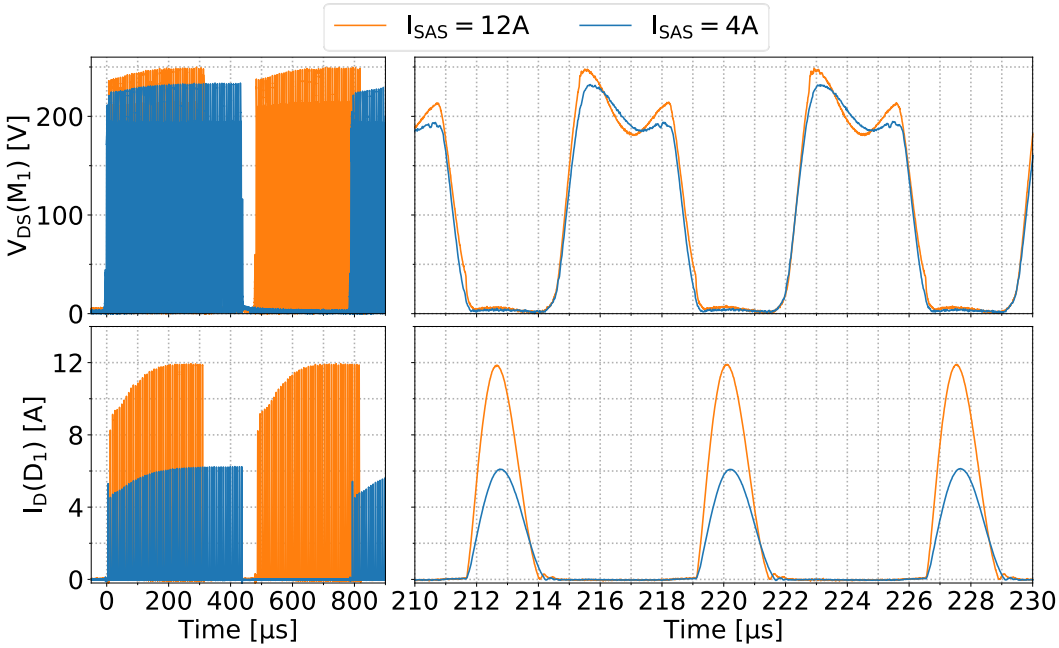

Figure 61. Experimental DCX waveform with MOSFET IXTQ42N25P for $\sum I_{SAS} = 4\ A$ (blue) and $\sum I_{SAS} = 12\ A$ (orange).
Top: Drain-Source voltage (M_1). Bottom: Rectifier diode current (D_1).

Table 16. Theoretical power losses at different values of $\sum I_{SAS}$ with MOSFET IXTQ42N25P (M_1, M_2)

$\sum I_{SAS}\ [A]$	4	12	Input current
$P_{Cr}\ [mW]$	46	415	Resonant capacitor losses
$P_{cond}\ [W]$	2,13	65,1	FET conduction losses
$P_d\ [W]$	2,05	10,0	Diode conduction losses
$P_{wn}\ [W]$	0,28	2,55	Winding conduction losses
$P_{hys}\ [W]$	13,52	13,52	Transformer hysteresis losses
$P_{DCX}\ [W]$	18,03	91,59	Overall power losses
$\eta\ [\%]$	95,49	92,37	Efficiency

Table 17. Main parameters from selected WBG FETs and Si MOSFET.

Component	IXTQ42N25P	SCTW90N65G2V	UJ4C075018K3S	TP65H035G4WSQA
Manufacturer	IXYS	STM	Qorvo	Transphorm
Technology	Si	SiC	SiC Cascode	GaN Cascode
$V_{DS}\ [V]$	250	650	750	650
$I_D\ [A]$ $(T_j = 100\ ºC)$	27	90	60	33
$r_{on}\ [m\Omega]$ $(T_j = 25\ ºC)$	84	18	18	35
$r_{on}\ [m\Omega]$ $(T_j = 100\ ºC)$	147	20	27	53
$Q_g\ [nC]$	100	120	38	31
$C_{oss}\ [pF]$	350	500	200	580

Since each device has a different C_{oss}, a redesign of the DCX timing was performed considering similar t_{on}, with the objective of limiting the magnetic flux density, and adjusting t_{gap} to achieve ZVS. Given the influence of t_{on} in P_{hys}, ω_r is increased by reducing C_r from 0,5 µF to 0,33 µF, thereby reducing t_{on}.

Each component was validated experimentally and, as shown in Figure 62, the primary transistor M_1 voltage and the rectifier diode D_2 current confirm that the ZVZCS condition is achieved in all cases. An analysis of the switching time and I_{rms} values provided in Table 18 reveals that the Si MOSFET achieves the smallest t_{gap} and I_{rms}, while the SiC cascode shows the lowest value among the WBG options and is similar to the Si MOSFET. However, the lowest r_{on} is essential to reduce the power losses of the DCX.

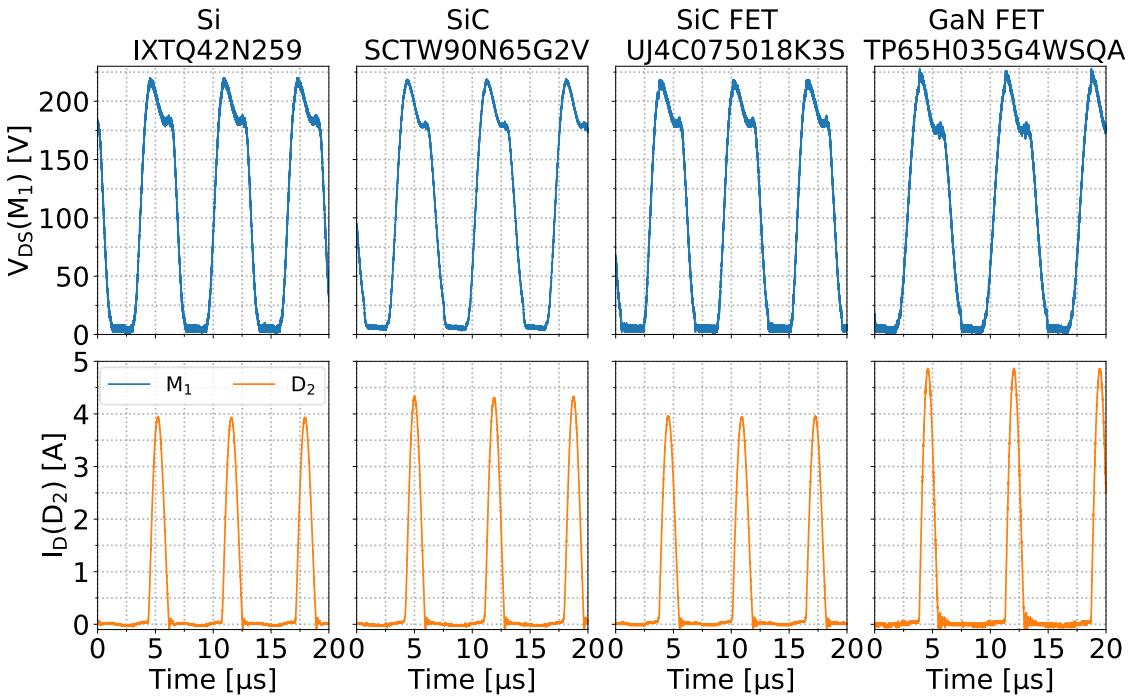

Figure 62. Experimental DCX waveforms for different transistors at $\Sigma I_{SAS} = 4\ A$. Top: Drain-Source voltage (M_1). Bottom: Rectifier diode (D_2).

Table 18. DCX timing and RMS currents using different transistors. Conditions: $C_r = 0{,}33\ \mu F$, $I_{SAS} = 4\ A$.

Component	IXTQ42N25P	SCTW90N65G2V	UJ4C075018K3S	TP65H035G4WSQA
$t_{on}\ [\mu s]$	1,91	1,90	1,90	1,83
$t_{gap}\ [\mu s]$	1,24	1,54	1,31	1,94
$f_{sw}\ [kHz]$	159	145	156	133
$I_{D_{rms}}\ [A]$	2,04	2,07	2,05	2,22
$I_{M_{rms}}\ [A]$	6,12	6,21	6,15	6,54

Taking the SiC cascode as a reference, due to its low r_{on}, the voltage waveform of the transistor M_1 and the current of the rectifier diode D_2 for $\Sigma I_{SAS} = 4\ A$ and $\Sigma I_{SAS} = 10\ A$ are represented in Figure 63. At higher currents, the ZVS conditions worsen and v_{on} increases from 15,1 V to 30,1 V. Simultaneously, the peak-to-peak voltage ripple of C_r increases from 35 V to 88 V, and the maximum peak voltage increases from 214 V to 245 V.

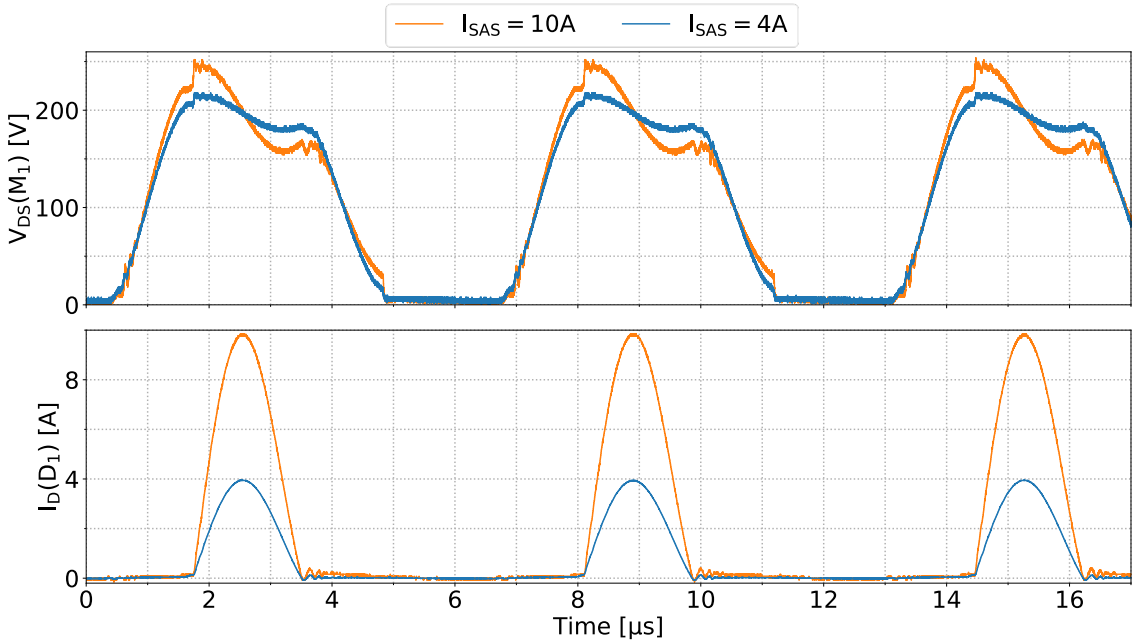

Figure 63. Experimental DCX waveform with SiC FET UJ4C075018K3S for $I_{SAS} = 4\ A$ (blue) and $I_{SAS} = 10\ A$ (orange).
Top: Drain-source voltage (M_1). Bottom: Rectifier diode current (D_1).

The efficiency for each semiconductor was measured as shown in Figure 64. DCX with Si MOSFET, despite having the lowest I_{RMS}, has the lowest overall efficiency, with a peak value of 96,5 % and drops significantly at higher currents with a minimum of 92,1 %, due to its large r_{on} and significant variation at high junction temperatures. In contrast, the SiC cascode achieved the highest efficiency with a peak value of 97,0 % and a minimum of 95,5 % at higher currents, thanks to its low r_{on} and C_{oss}. Meanwhile, the GaN cascode, due to its high C_{oss}, showed efficiencies similar to the Si MOSFET, with a peak value of 96,5 % and a minimum of 94,3 %.

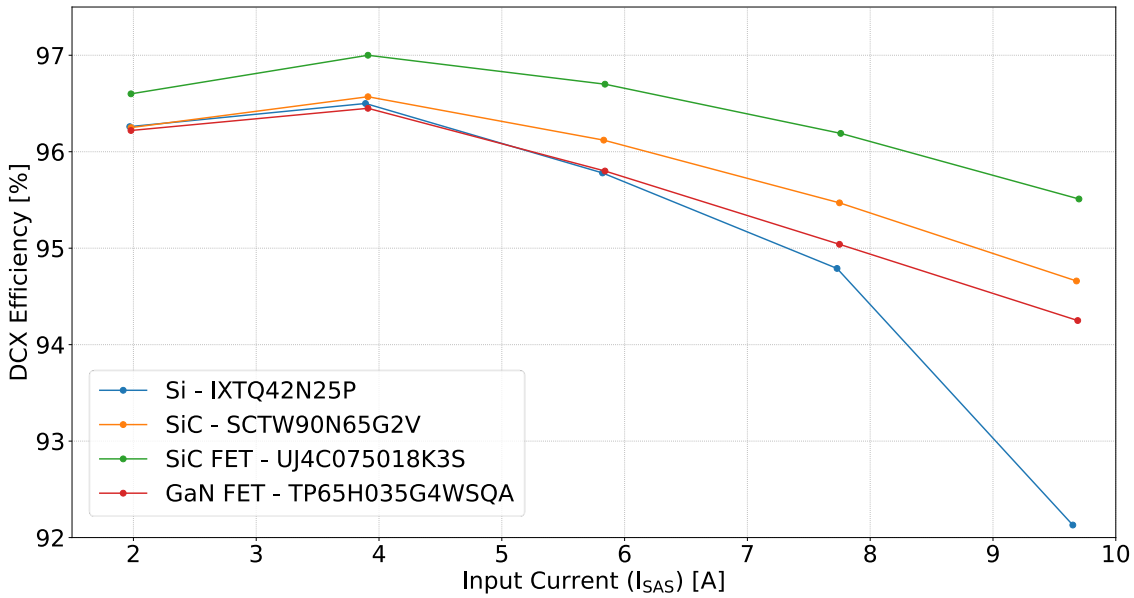

Figure 64. DCX efficiency with different transistor technologies.

As a potential replacement for existing S3R systems, the efficiency of the proposed S3DCX has been compared with commercial products, please refer to Table 19. Although the efficiency of the S3DCX is lower, it should be noted that it adds other important benefits, such as the ability to serialise outputs to achieve higher bus voltages.

Table 19. Power characteristics of commercial modules PCU and proposed S3DCX

Model	S3DCX (SiC Cascode)	PSR100V [175]	PCU NG [176], [177]	APSTAR-6E [178]
Regulation	S3DCX	S3R	S3R	S3R
Power [kW]	1	1,35	1,6	2,0
Efficiency [%]	97,0	98,8	99,0	99,0

4.4.3 Design for *n x m* power cells with output series connection

Output series connection of power cells can be used to increase V_{BUS}, but as presented in section 3.4.2, the I-V curves of the solar array sections must be similar to ensure voltage equalisation. As illustrated in Figure 65, the S3DCX in output series configuration can be

seen as an $n \times m$ matrix of power cells, where n represents the number of output series power cells and m denotes the number of strings in parallel connected to the bus.

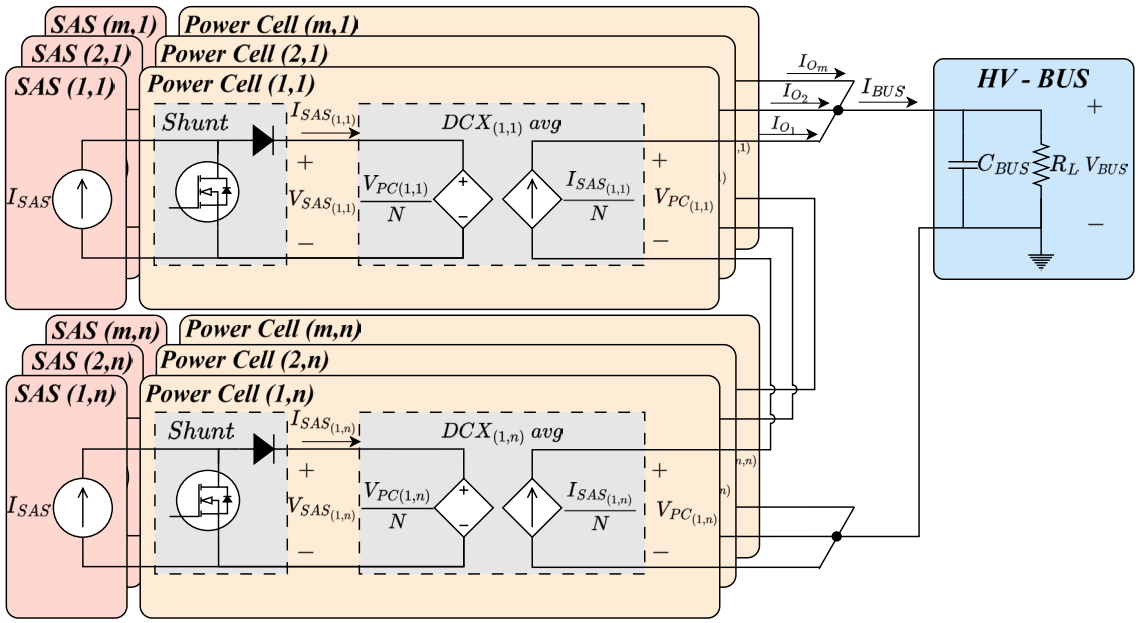

Figure 65. Generalized S3DCX with *m* strings and *n* output power cells in series

In series output connection, V_{BUS} is defined as the sum of the output voltage of the power cells, V_{PC}, (61). However, this does not imply an equal voltage distribution between the power cells, which depends on the actual operating point of each SAS. In the ideal case, where all SAS supply the same current $I_{SAS1} = I_{SAS2} = \cdots = I_{SASm}$, it can be assumed that I_{BUS} is given by (62). Since V_{BUS} is simply the sum of V_{PC} and the DCX provides galvanic isolation, the serialisation of the power cells does not affect the individual design of each power cell, which can be treated as an independent element.

$$V_{BUS} = \sum_{i=1}^{n} V_{PC_i} = N \cdot \sum_{i=1}^{n} V_{SAS_i} \tag{61}$$

$$I_{BUS} = \sum_{i=1}^{m} I_{O_i} = \frac{1}{N} \cdot \sum_{i=1}^{m} I_{SAS_i} \tag{62}$$

In series connection, the maximum current delivered by the string is limited by the SAS with the lowest I_{SC}, thereby limiting the power generated by the other SAS in the string. Therefore, in a string, $N \cdot V_{OC}$ of each SAS must be greater than V_{BUS} to ensure power transfer to the bus (63).

$$V_{BUS} < N \cdot \sum_{i=1}^{n} V_{OC_i} \tag{63}$$

For the S3R control loop design, the minimum bus capacitance, C_B, and the voltage loop bandwidth, ω_{BW} can be adapted using equations (61) and (62), resulting in (64) and (65).

$$\omega_{BW} = \frac{1}{R_L C_B} = \frac{I_{BUS}}{V_{BUS} C_B} = \frac{\sum_{i=1}^{m} I_{SAS_i}}{C_B N^2 \sum_{i=1}^{n} V_{SAS_i}} \tag{64}$$

$$C_B \geq \frac{I_{BUS}}{400\pi V_{BUS}} = \frac{\sum_{i=1}^{m} I_{SAS_i}}{400\pi \cdot N^2 \sum_{i=1}^{n} V_{SAS_i}} \tag{65}$$

The other S3R control loop equations are modified as follows: voltage divider, k, (66), maximum output impedance (67) and bus voltage ripple $\Delta V_{BUS|pp}$ (68). The maximum allowable values defined in ECSS-E-ST-20C [6] for the maximum output impedance in section 5.7.2.o and the maximum $\Delta V_{BUS|pp}$ in section 5.7.2.m are given by (69) and (70), respectively.

$$k = \frac{V_{ref}}{V_{BUS}} = \frac{V_{ref}}{N \sum_{i=1}^{n} V_{SAS_i}} \tag{66}$$

$$|Z_o(s)|_{max} = \frac{1}{G k k_p} = \frac{N \sum_{i=1}^{n} V_{SAS_i}}{V_{ref} G k_p} \tag{67}$$

$$\Delta V_{BUS|pp} = \frac{V_C V_{BUS}}{V_{ref} k_p} = \frac{V_C N \sum_{i=1}^{n} V_{SAS_i}}{V_{ref} k_p} \tag{68}$$

$$|Z_o(s)|_{max} \leq 0{,}02 \frac{V_{BUS}}{I_{BUS}} = 0{,}02 \frac{N^2 \sum_{i=1}^{n} V_{SAS_i}}{\sum_{i=1}^{m} I_{SAS_i}} \tag{69}$$

$$0{,}5 \cdot 10^{-2} V_{BUS} \geq \frac{V_C V_{BUS}}{V_{ref} k_p} \tag{70}$$

Regarding the PI controller parameters, the equation (70) can be rearranged to determine the minimum value of k_p as shown in (71). In addition, k_i is influenced by the increase in V_{BUS}, which degrades the margin phase and potentially leads to instability in the control loop (72).

$$k_p \geq \frac{200 \cdot V_C}{V_{ref}} \tag{71}$$

$$k_i \leq k_p \cdot \frac{\omega_{BW}}{10} = 4 \cdot 10^3 \frac{V_C I_{BUS}}{C_B V_{ref} V_{BUS}} = 4 \cdot 10^3 \frac{V_C \sum_{i=1}^{m} I_{SAS_i}}{C_B V_{ref} N^2 \sum_{i=1}^{n} V_{SAS_i}} \tag{72}$$

Finally, it is necessary to synchronise each power cell within each string. In practice this has been achieved by sharing the hysteresis comparator between all the serialised power cells.

4.4.4 Digital driving circuit

During the vacuum and partial pressure experiments, the power cell was operated in open-loop mode, digitally controlled by a Field-Programmable Gate Array (FPGA), specifically the Lattice Semiconductor iCE40HX-1k model. For simplicity, the FPGA generated two fixed duty cycle Pulse Width Modulation (PWM) to drive the shunt M_{sh} and the DCX, M_1 and M_2.

The digital power cell driving circuit is shown in Figure 66 and the code is available in Annex V. A Phase-Locked Loop oscillator (PLL) generates a 100,5 MHz clock signal with a resolution of 9.95 ns. This clock feeds a digital counter which sets $t_{dr\ on}$ and $t_{dr\ gap}$ and the shunt transistor timing signals, $t_{sh\ on}$ and $t_{sh\ off}$ drive signals. To avoid high frequency noise during the shunt interval, M_1 and M_2 are disabled when M_{sh} is active. A synchronous module works in a similar way to a demultiplexer. It alternates the drive signals between M_1 and M_2. Instead of incorporating a selector input, the falling edge of the received pulses is detected and the signal alternates between the outputs with each received pulse. The resulting waveforms are displayed in Figure 67.

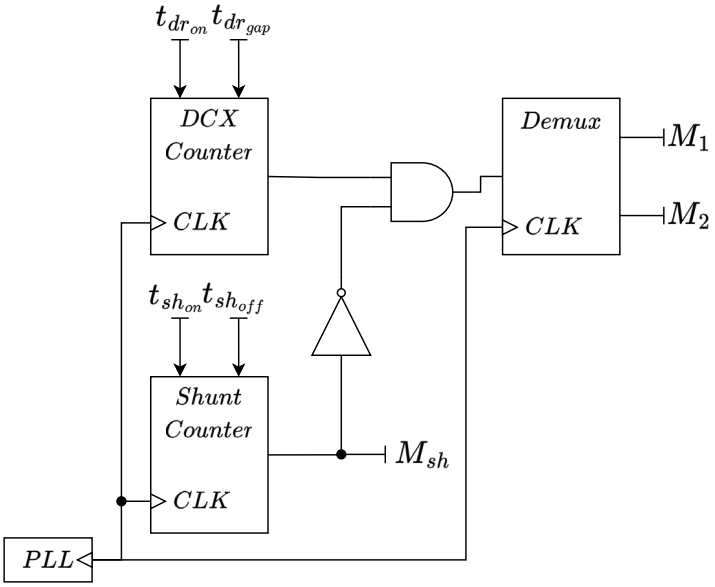

Figure 66. Circuit schematic for digital driving.

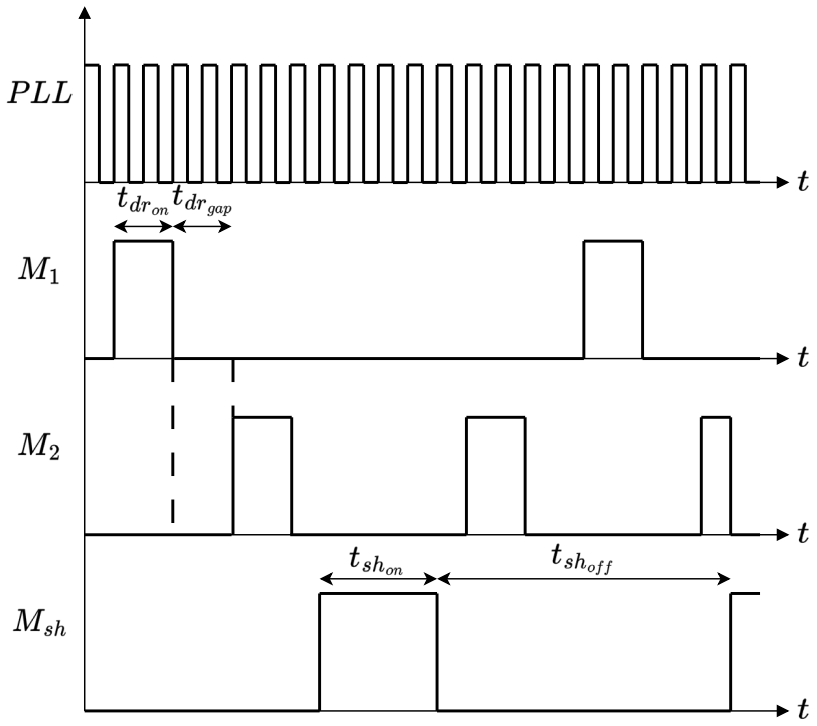

Figure 67. Driving waveforms for the DCX and shunt section from digital control.

4.5 Partial conclusions

This chapter has presented, analysed, and extended the results of the article *"Enabling high-power conditioning and high-voltage bus integration using series-connected DC transformers in spacecrafts"* [30]. The main contribution of the article is the development of a solution to achieve HV distribution buses based on the serialisation of power cells using the S3DCX architecture. This is intended for high power space platforms such as SBSP. The proposed concept has been modelled and experimentally validated with 400 W, 3:1 voltage ratio and 100 V SAS. Regulated distribution buses of 600 V and 900 V have been successfully demonstrated.

A review of FETs and diodes, including WBG semiconductors, has been undertaken to assess their compatibility with application requirements in terms of performance and radiation tolerance. In conclusion, SiC Schottky diodes require significant voltage derating to avoid SEB and further development is necessary to enhance their reliability.

The performance and operation of the DCX converter has been analysed and validated for high current SAS, up to 10 A. At high power, the efficiency drops mainly due to the conduction losses, while magnetic core losses remain unchanged. To improve the efficiency, several types of WBG FETs have been analysed. Among these, SiC cascode FETs demonstrated a notable efficiency improvement, reaching a maximum of 97,0 %.

The output series connection of power cells has been modelled. Although the S3R control loop provides voltage regulation, with different SAS I-V curves, the output voltage of each power cell will be unbalanced. The SAS with the lowest I_{SC} will limit the current of the rest of the SAS. The control loop modifications required for output series connection of power cells have also been detailed.

Several tests have been carried out to evaluate the electrical isolation of the transformer and its reliability under partial pressure conditions. The functionality of the power cell has been validated under high-vacuum conditions and the component identification susceptible to arcing under partial pressure conditions has been performed. Digital driving signals have been also validated for these tests.

Chapter 5

Contributions, conclusions and future lines of work

5.1 Contributions

The following sections describe the main contributions of the present thesis.

5.1.1 Article I: Sequential switching shunt regulation using DC transformers for solar array processing in high voltage satellites

The first article [132] presented in this thesis, whose results and the discussion are detailed in Chapter 3 has contributed to:

1. **Description of a modular solar array regulator, devised for spacecraft high voltage distribution buses**: **S3DCX**. This solar array regulator combines two techniques, the current-fed ZVZC isolated converter working as a DCX and the S3R control loop for voltage regulation.

2. **Design methodology** for the S3DCX and its control loop based on the **ECSS standard**. A software tool was provided to help with the design.

3. **Implementation of a 2 kW prototype** based on five 400 W power cells with 100 V input voltage and 300 V output voltage.

4. **Technology Readiness Level 4 validation.** Successful evaluation under different operating conditions and power cell configurations, including output series connection, in accordance with ECSS requirements.

5.1.2 Article II: Enabling high-power conditioning and high-voltage bus integration using series-connected DC transformers in spacecrafts

The second article [30] presented in this thesis, whose results and discussion are detailed in Chapter 4 has contributed to:

1. **Identification of DC voltage levels for very high power space applications** based on actual ECSS output impedance requirements.
2. **Comparative analysis of commercial-of-the-shelf (COTS), WBG power semiconductors** for their use in HV, high power space applications. For SiC power devices, 300 V was identified as the maximum value for safe operation against SEB.
3. **Implementation of 1,0 kW S3DCX power cells (10 A, 100 V)** using WBG semiconductors. Of the power semiconductors tested, SiC Cascode power devices demonstrated the highest efficiency.
4. **Control loop generalisation for the S3DCX series – parallel configuration** to accommodate very high voltage bus.
5. **S3DCX validation for 600 V and 900 V bus voltage** using 300 V output series connected power cells and under balanced and unbalanced SAS.
6. **S3DCX validation under partial and high vacuum conditions.**

5.2 Conclusions

Taking into consideration the results obtained, and the knowledge gained during the development of this thesis, a number of conclusions have been reached in relation to the research question. These conclusions are listed below:

1. **The maximum voltage of 120 V in the solar arrays imposes a limit on the conventional DET architecture**, which restricts the maximum power of the spacecraft to 30 kW. Despite dedicated efforts to increase the operating voltage

of photovoltaic sources, the occurrence of HV effects degrades the solar cells, thus limiting their viability in the medium term.

2. **New architectures will be required to enable HV buses from LV solar arrays** to supply high power satellites. It is concluded that 900 V DC is the most suitable for 1 MW space power systems, such as the proposed SBSP prototypes.

3. **Dual bus architectures considering LV and HV buses will be required for high power spacecraft**. The LV bus would be used for platform systems and low power payloads, while the HV bus would be dedicated to high power payloads.

4. **The S3DCX, a novel DET architecture, is a promising candidate to HV buses,** capable of converting and regulating the voltage from 100 V SAS to a 300 V distribution bus, opening up the possibility of power distribution up to 180 kW as a baseline.

5. **The S3DCX facilitates output-series connection**, allowing the output voltage to be multiplied by the number of power cells connected in series without affecting the voltage rating of the individual power cells. Very high voltage DC buses, in the kV range, are possible with this approach, opening the door to SBSP applications.

6. **HV power buses will be possible if further technological advancements are made in power semiconductors**, which has been identified as a major issue for SEE.

7. **The S3DCX will facilitate the development of other high power applications** such as electric propulsion, space stations, microgrids….

5.3 Future lines of work

The findings of this thesis provide a series of future lines of work that will further mature the technology required for power conditioning and solar array regulation in high voltage space applications. The following sections describe several proposals that are considered to be of potential interest.

5.3.1 Increase of S3DCX power density

The 2 kW S3DCX prototype has a total weight of 4,4 kg, resulting in a power density of 454 W/kg. While the prototype was designed as a first technology demonstrator, achieving a higher TRL would require efforts in miniaturisation, mechanical and thermal design to increase the power density.

The use of WBG semiconductors, in particular GaN FETs or SiC FET cascodes with lower output capacitance, will allow higher switching frequency, a reduction in the magnetising inductance of the transformer and the resonant capacitor, and ultimately a more compact design. In addition, the use of planar transformers would result in a further reduction in volume while improving the consistency of the electrical parameters of the transformers. Other means of reducing t_{gap} can be explored to increase the effective duty cycle and reduce conduction losses. The incorporation of an auxiliary inductor, as suggested in [179], is worth exploring.

5.3.2 SEE in HV power semiconductors

The use of SiC JFETs in cascode and supercascode structures has been identified as a potential solution to mitigate SEB problems in HV devices.

5.3.3 Digital control

Although an analogue control loop provides a more robust implementation, it becomes challenging to incorporate complex algorithms when required. The adoption of digital processors will simplify the implementation of advanced control strategies.

Due to component tolerances, the switching timing of the DCX is manually adjusted during implementation in order to ensure correct ZVZCS during t_{on} and t_{gap}. However, temperature variations, degradation, or failure modes in the resonant capacitor can cause the resonant frequency to drift, resulting in the loss of the ZVZCS condition. Adaptive adjustment of the timing signals will be easier with digital control, as well as for power cell interleaving.

5.3.4 Study of new architectures based on the DCX

The S3DCX has been proven to be a viable option for SAS regulation in HV distribution buses. The flexibility of the S3DCX allows alternative architectures to be explored for different applications. Following the same principle that led to the design of the S3DCX, by combining the S3R for voltage regulation and the DCX for voltage conversion, the S3R could be replaced by an Sequential Switching Shunt Series Regulator (S4R) to connect directly the SAS to a battery for charging. In addition, the control loop of the S3DCX can be adapted with an MPPT algorithm to achieve an unregulated distribution bus while maximising power extraction from the SAS, as illustrated in Figure 68.

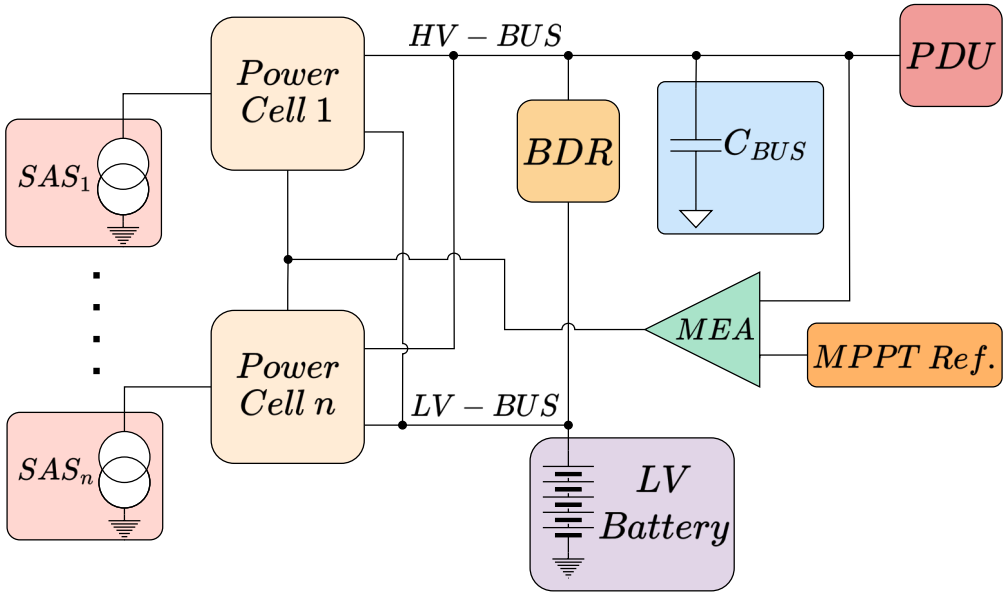

Figure 68. Proposal of an isolated S4R+MPPT architecture based on the S3DCX concept.

Moreover, the serialisation of the power cells allows for the implementation of a bipolar distribution bus, with the centre tap between the outputs of the power cells acting as the ground reference, as represented in Figure 69. This configuration provides two independent distribution buses that can be interconnected to form a third bus with double the voltage. The implementation of a bipolar bus system has the potential to be beneficial for inverter based applications, particularly for the control and operation of high power motors.

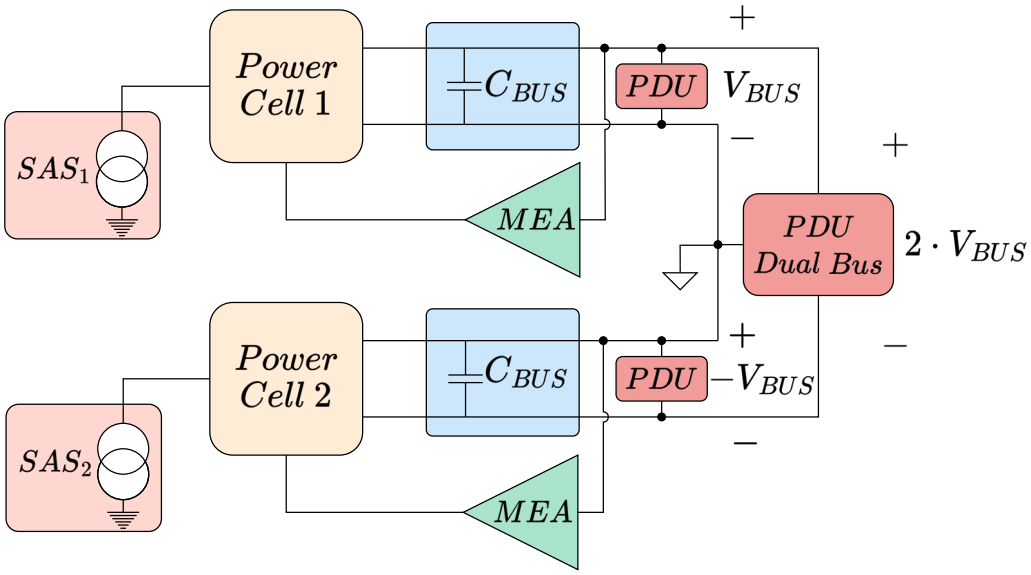

Figure 69. Proposal of bipolar bus architecture based on the S3DCX concept.

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Annex I

Schematic of S3DCX prototype

In this annex is presented the schematics used for the implementation of the S3DCX used in Chapter 3 and Chapter 4.

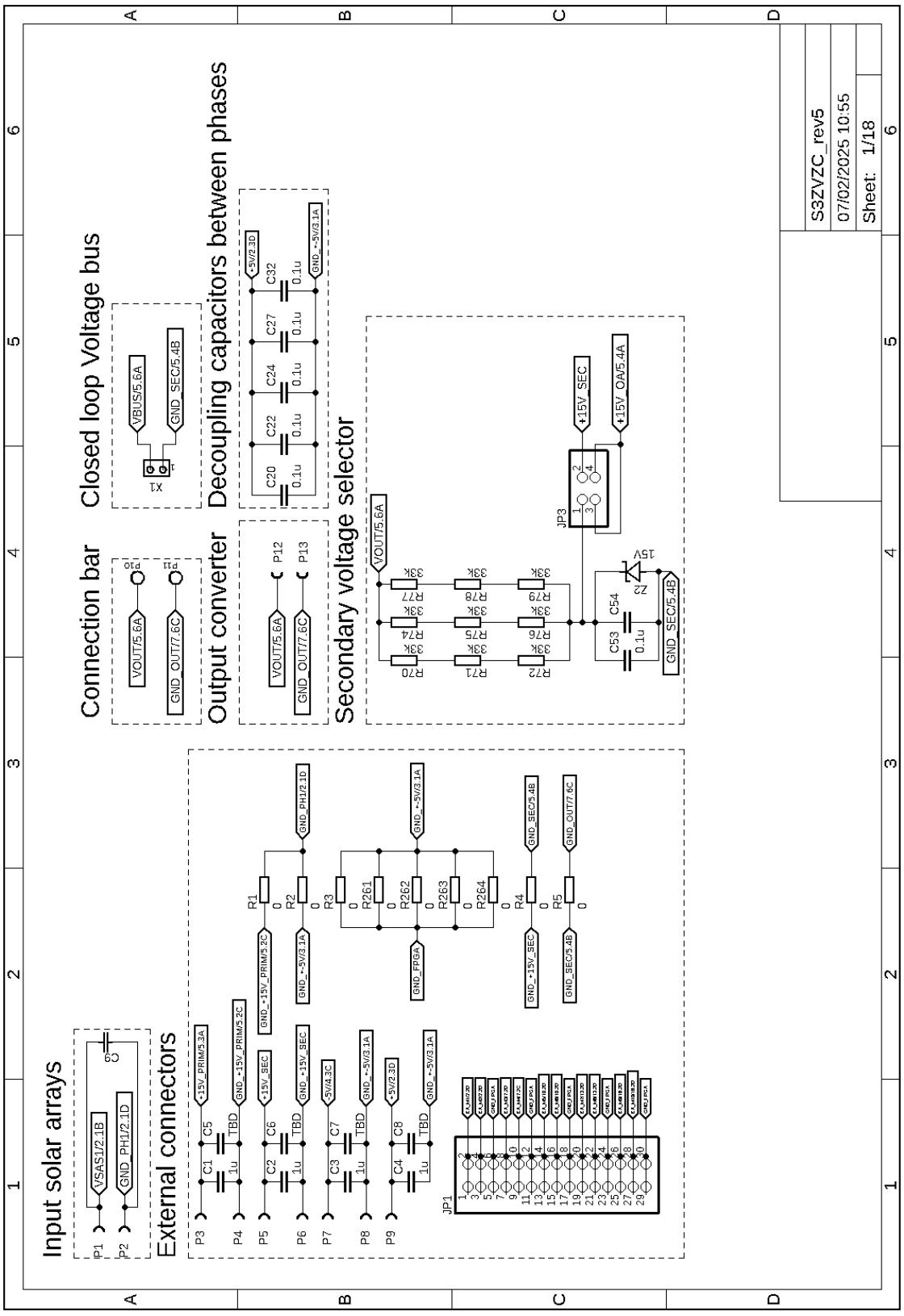

Figure 70. S3DCX prototype schematic – General connectors.

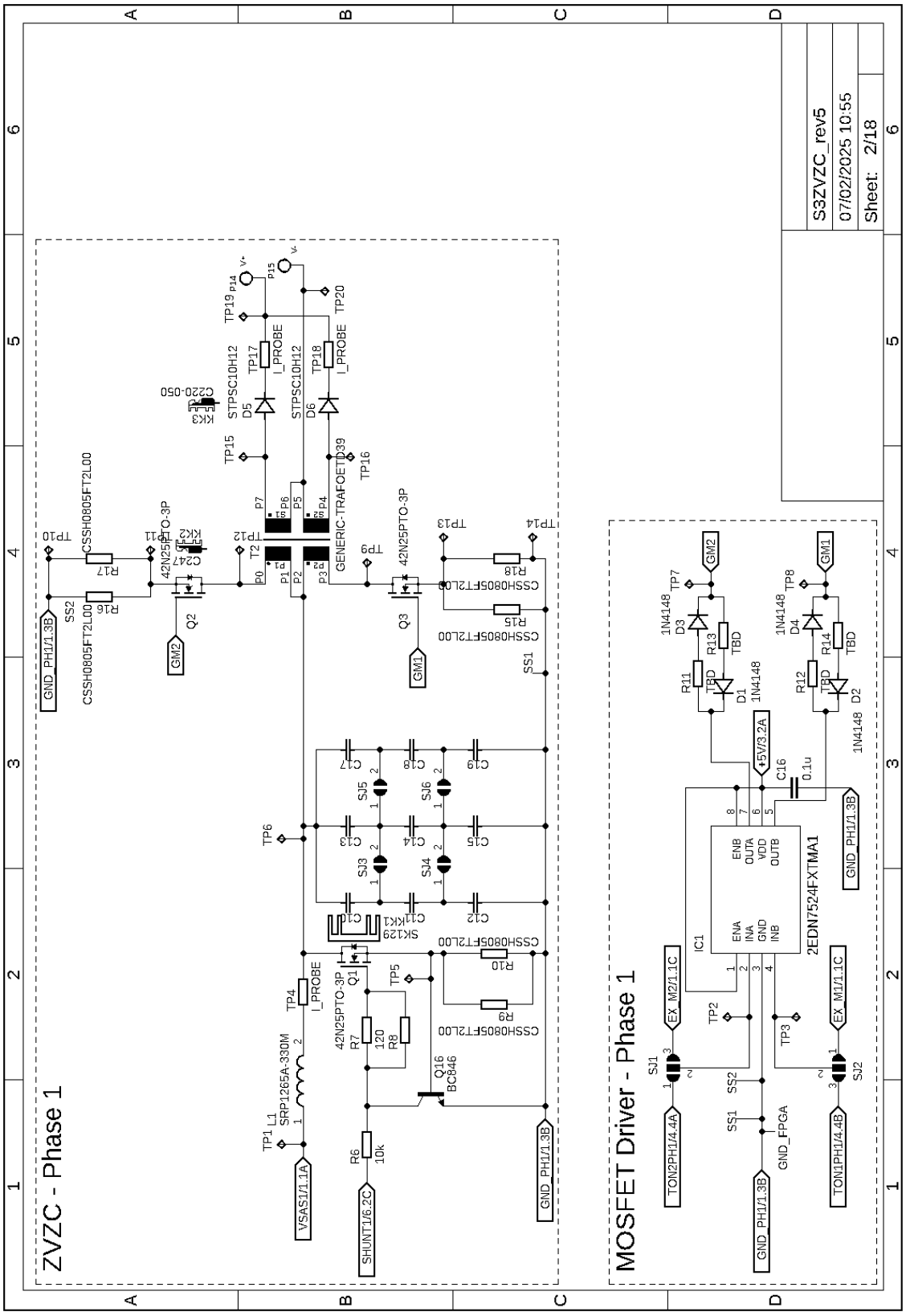

Figure 71. S3DCX prototype schematic – Power cell phase 1.

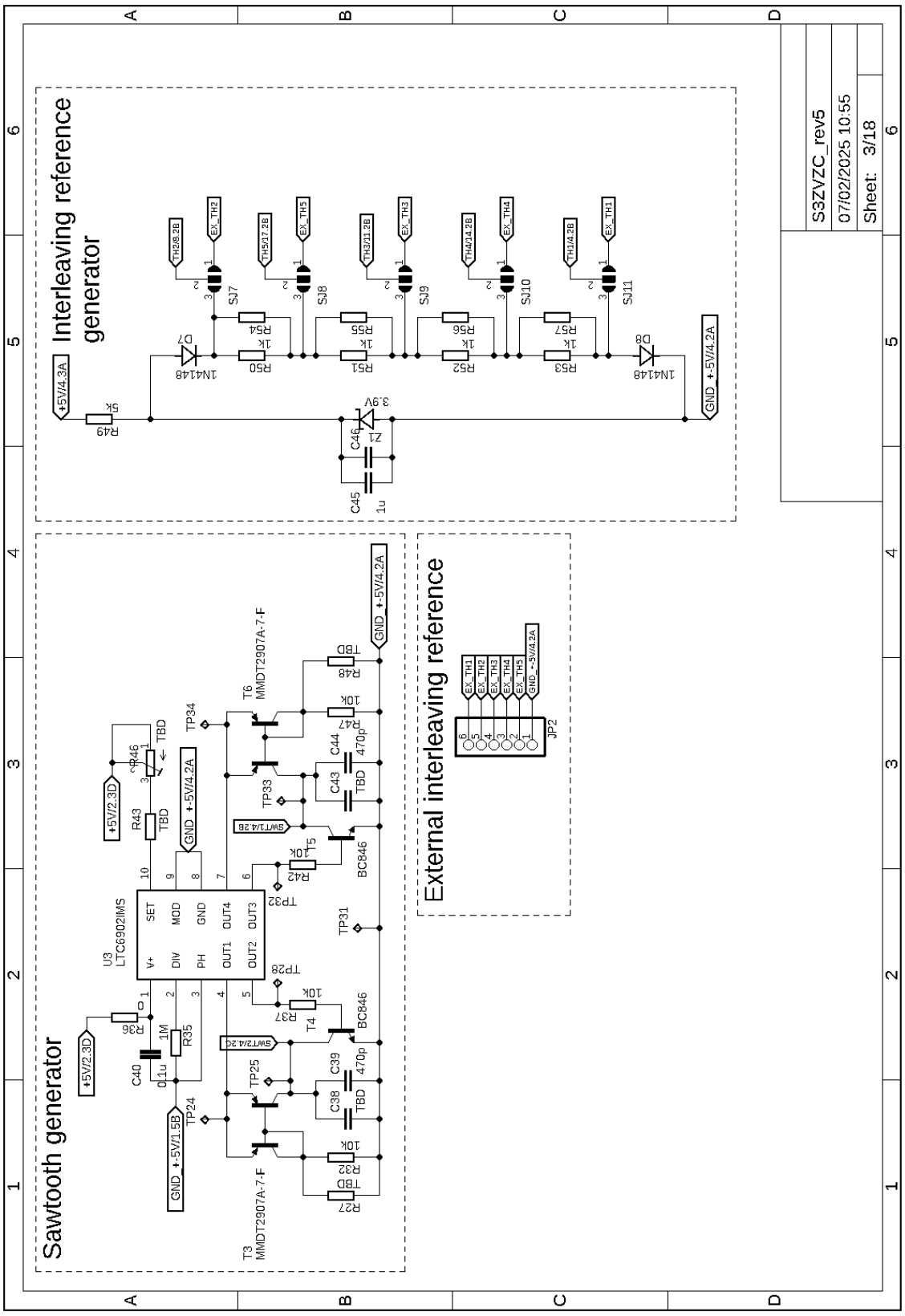

Figure 72. S3DCX prototype schematic – Common driving circuit.

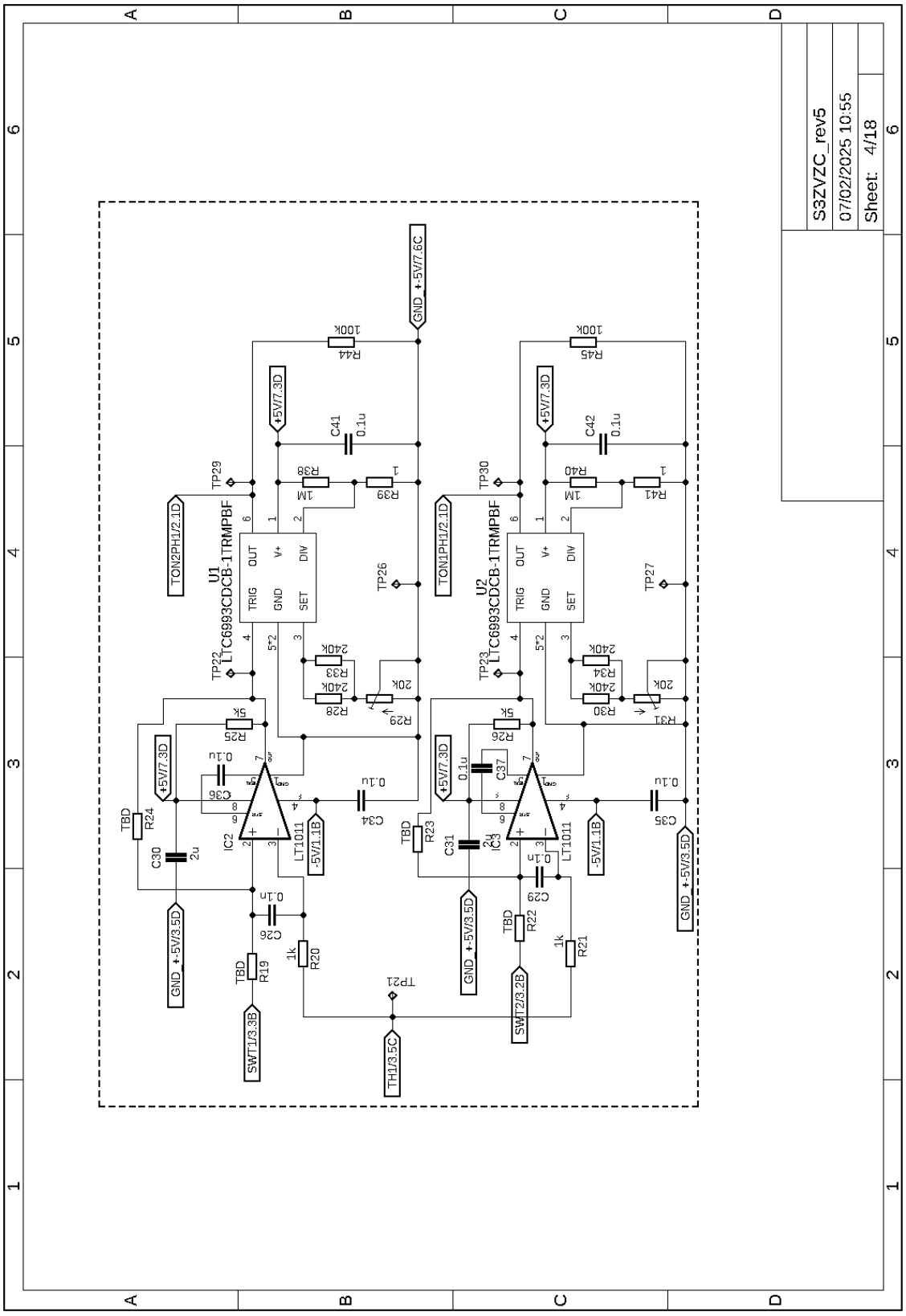

Figure 73. S3DCX prototype schematic – Time pulse phase 1.

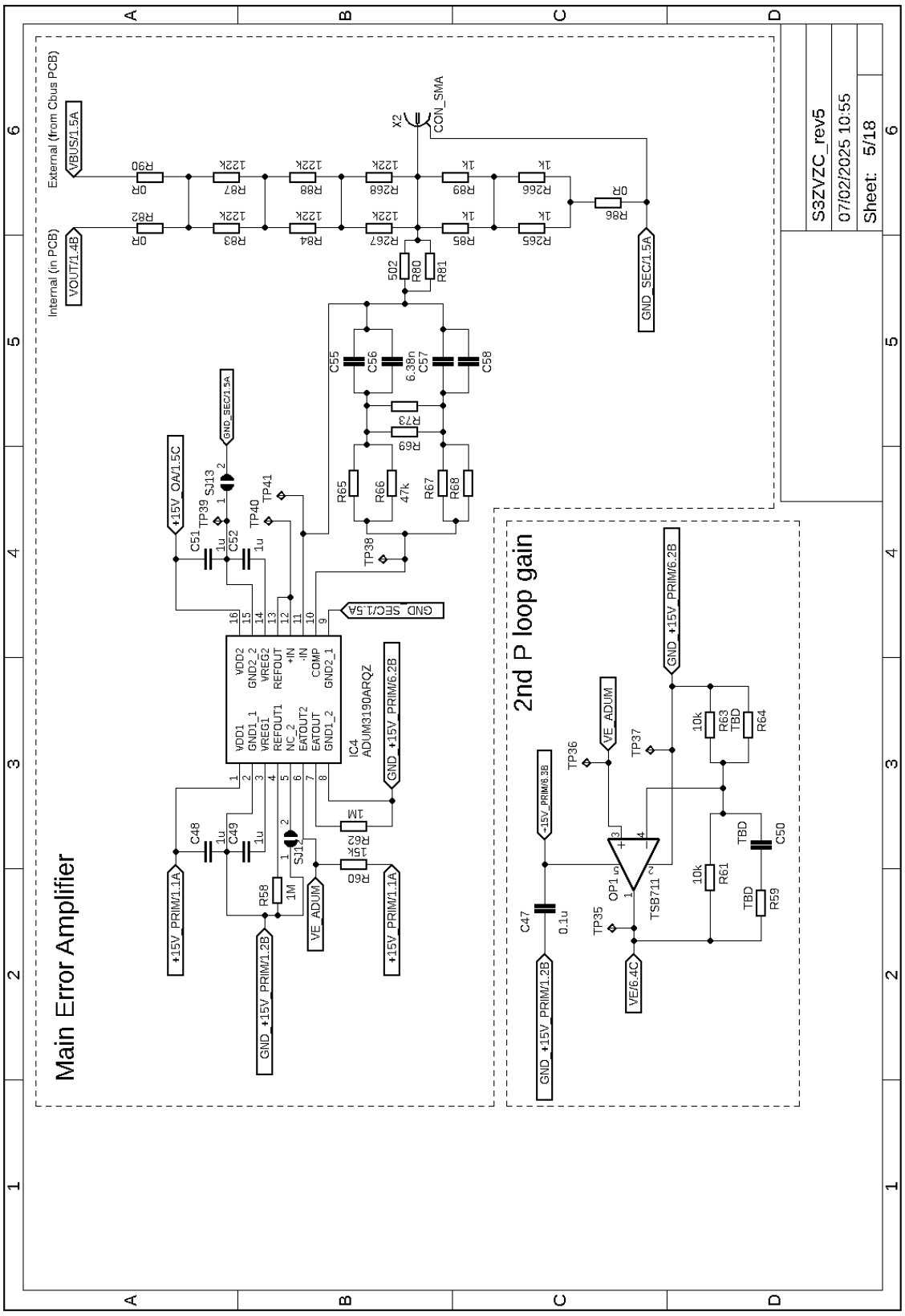

Figure 74. S3DCX prototype schematic – Main Error Amplifier.

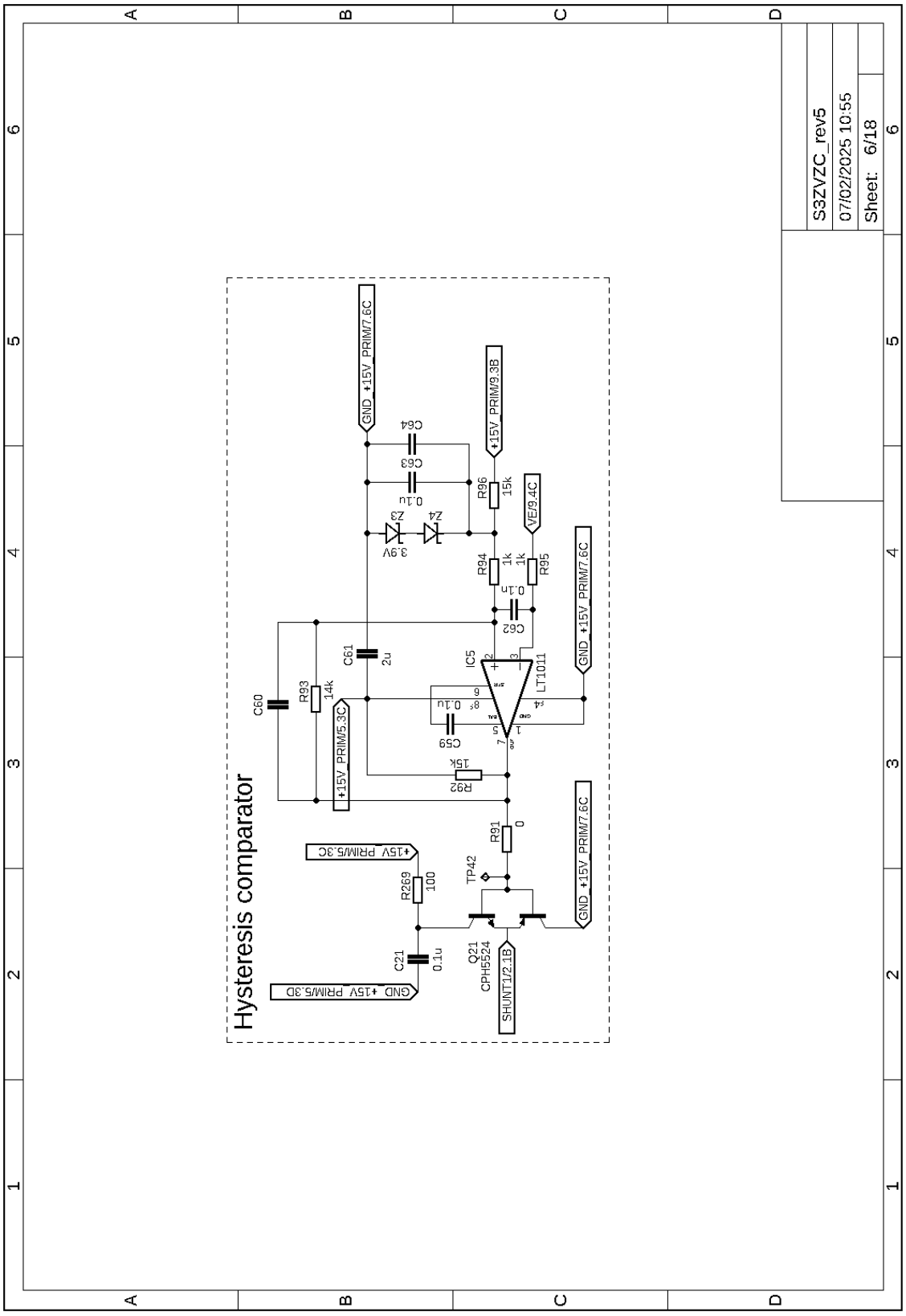

Figure 75. S3DCX prototype schematic – Hysteresis comparator phase 1.

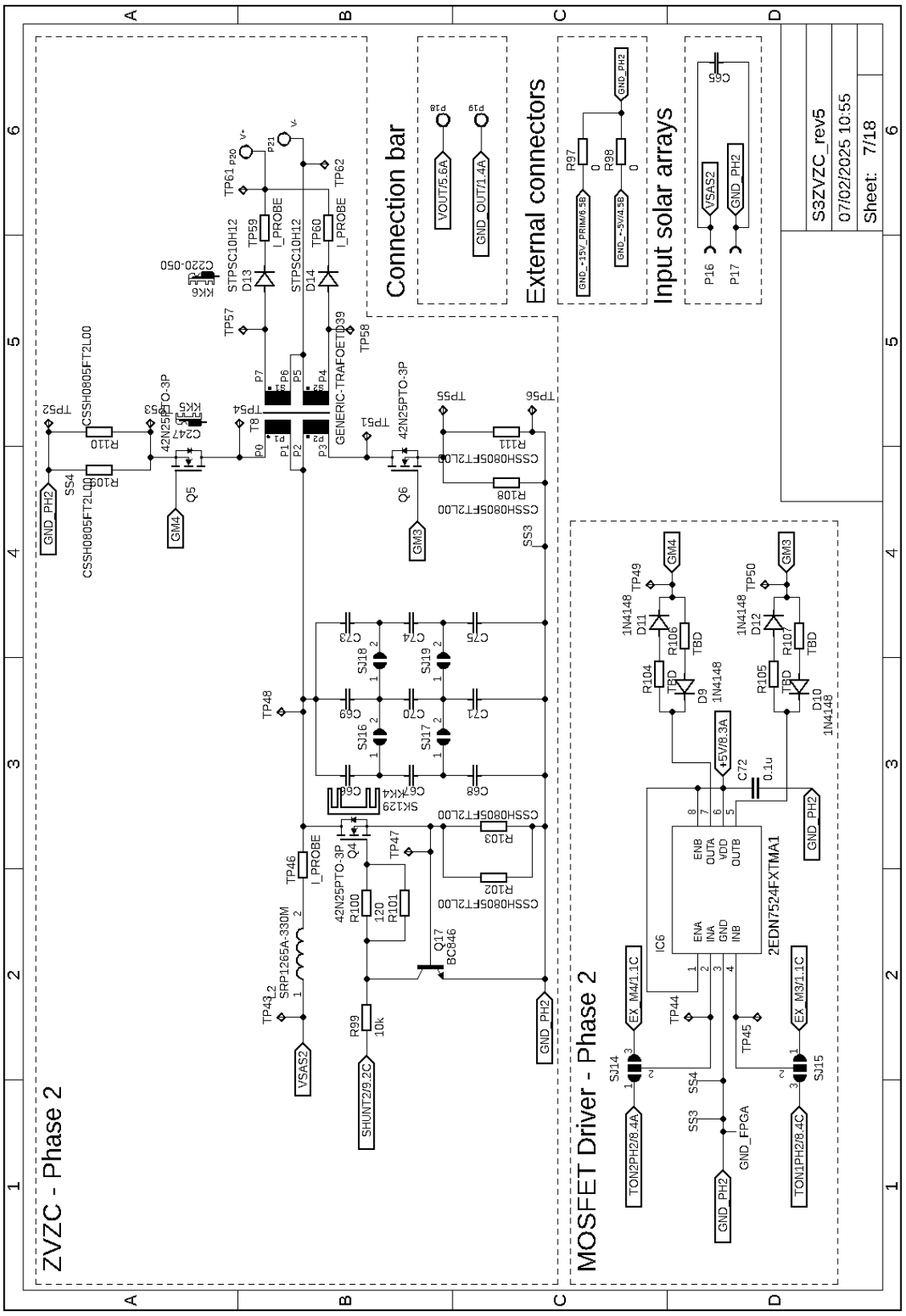

Figure 76. S3DCX prototype schematic – Power cell phase 2.

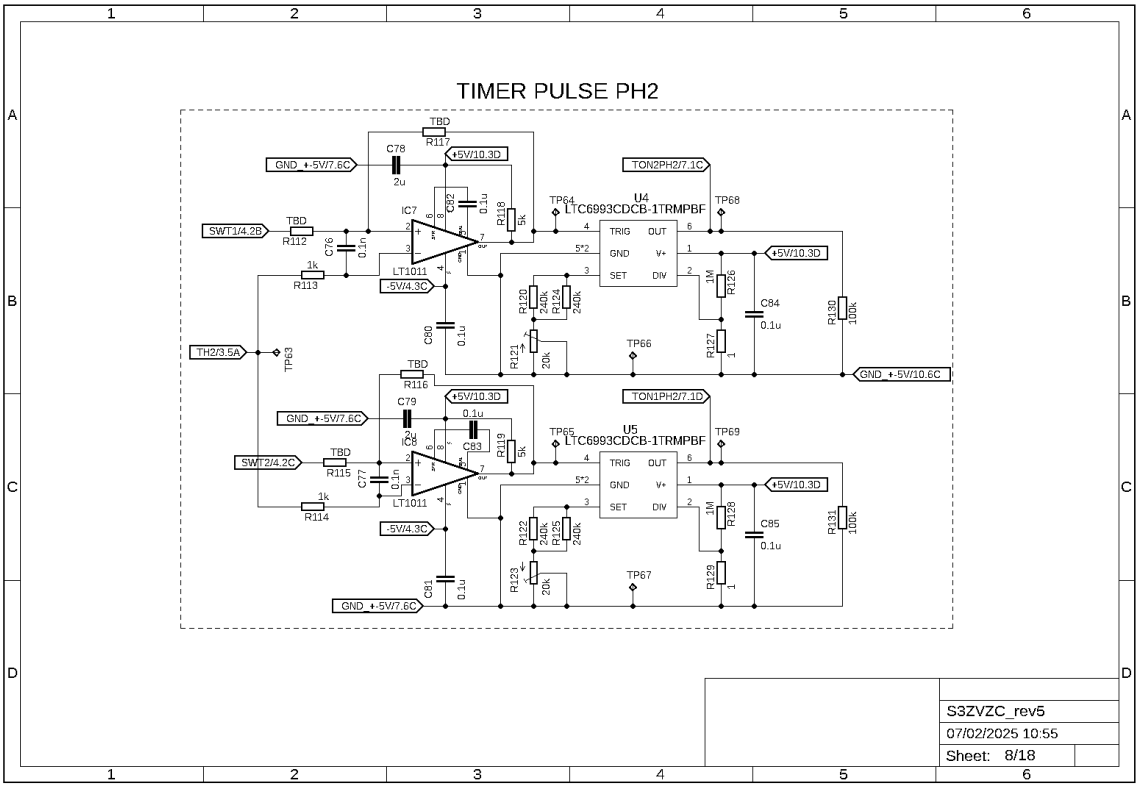

Figure 77. S3DCX prototype schematic – Timer pulse phase 2.

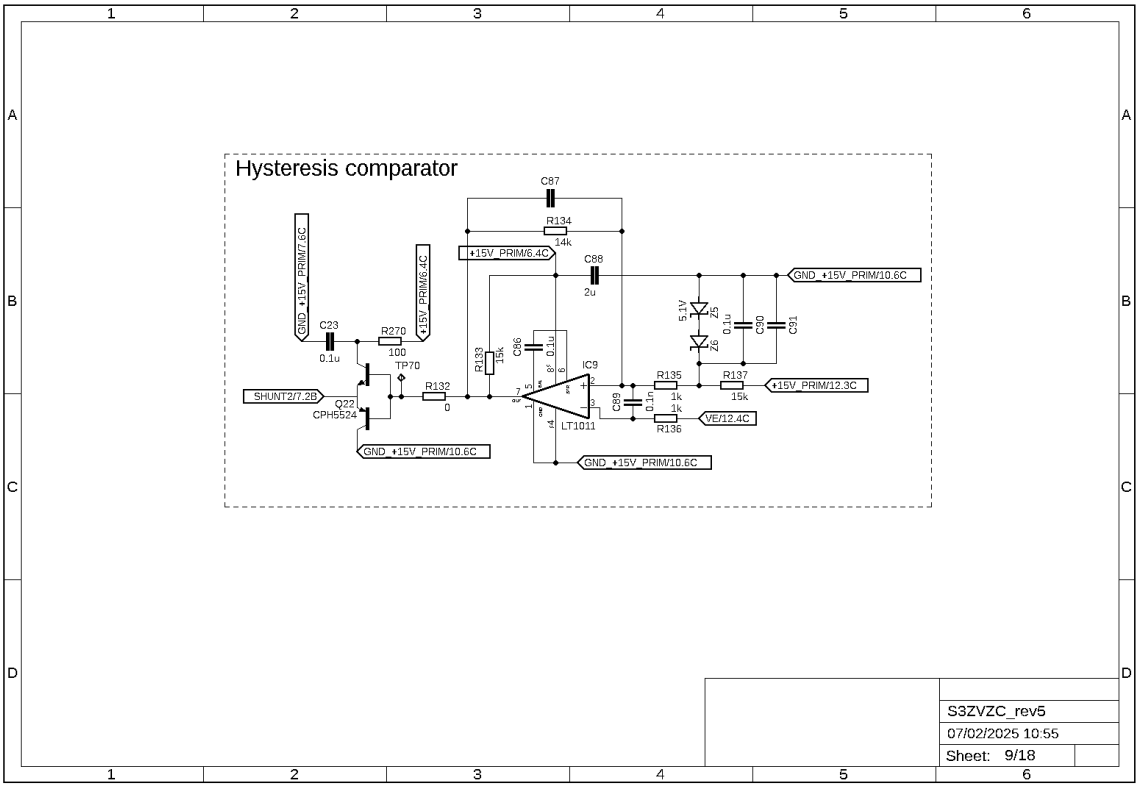

Figure 78. S3DCX prototype schematic – Hysteresis comparator phase 2.

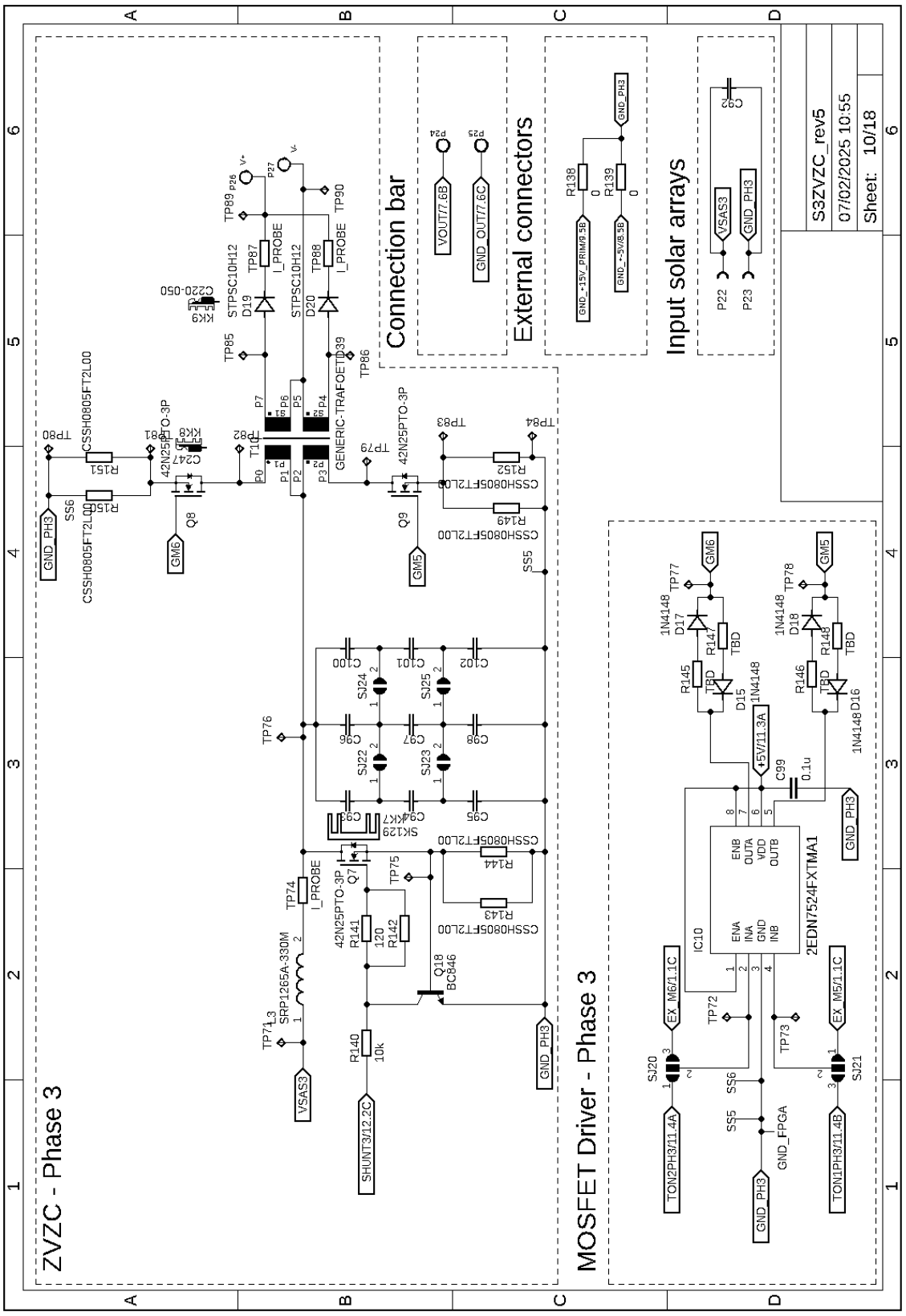

Figure 79. S3DCX prototype schematic – Power cell phase 3.

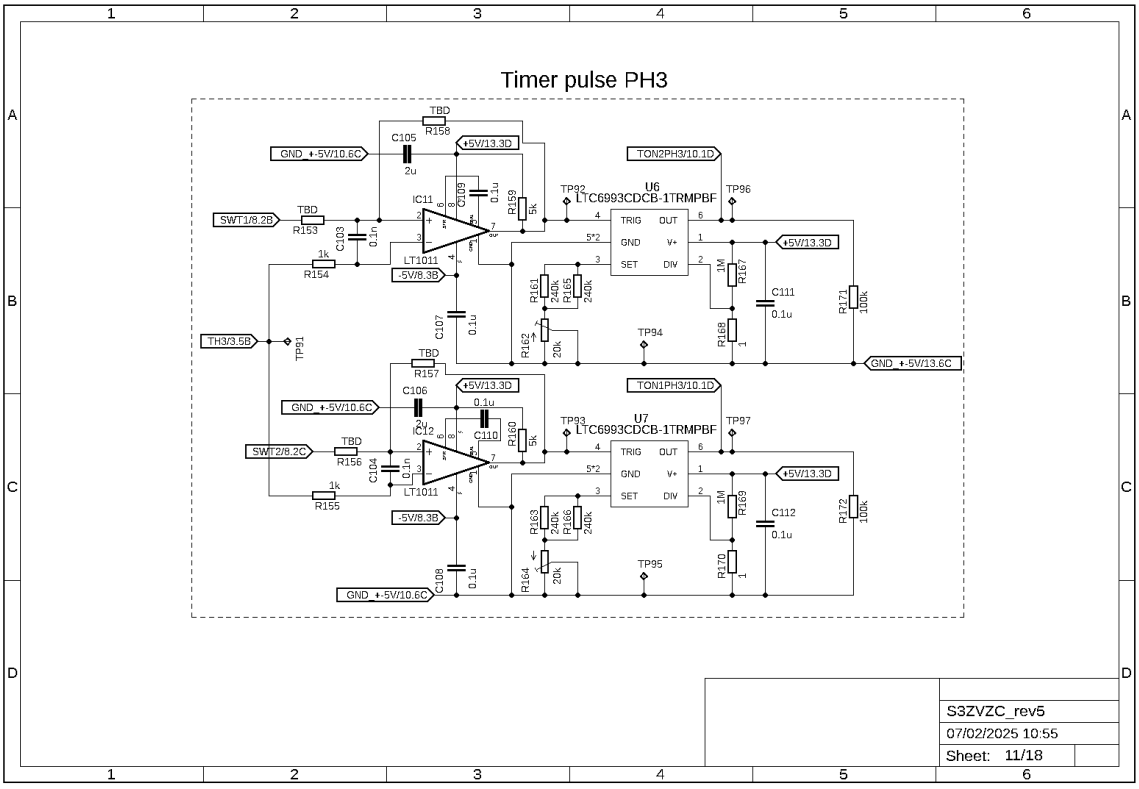

Figure 80. S3DCX prototype schematic – Timer pulse phase 3.

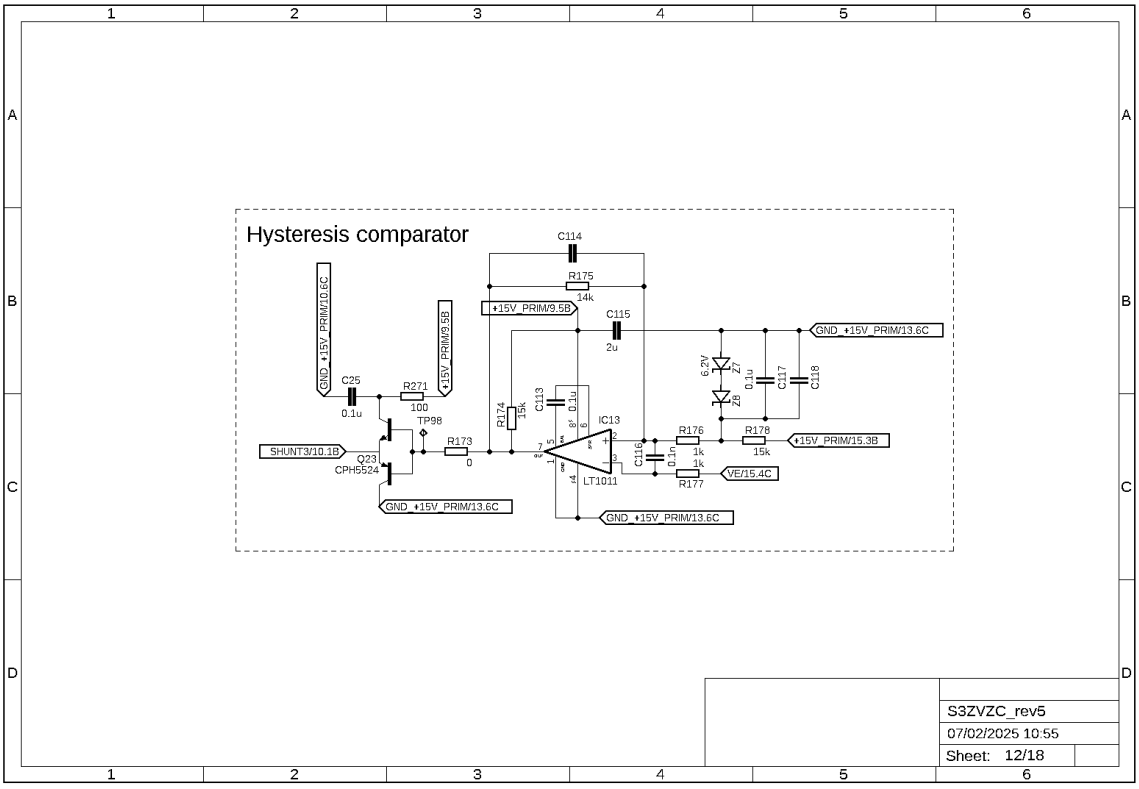

Figure 81. S3DCX prototype schematic – Hysteresis comparator phase 3.

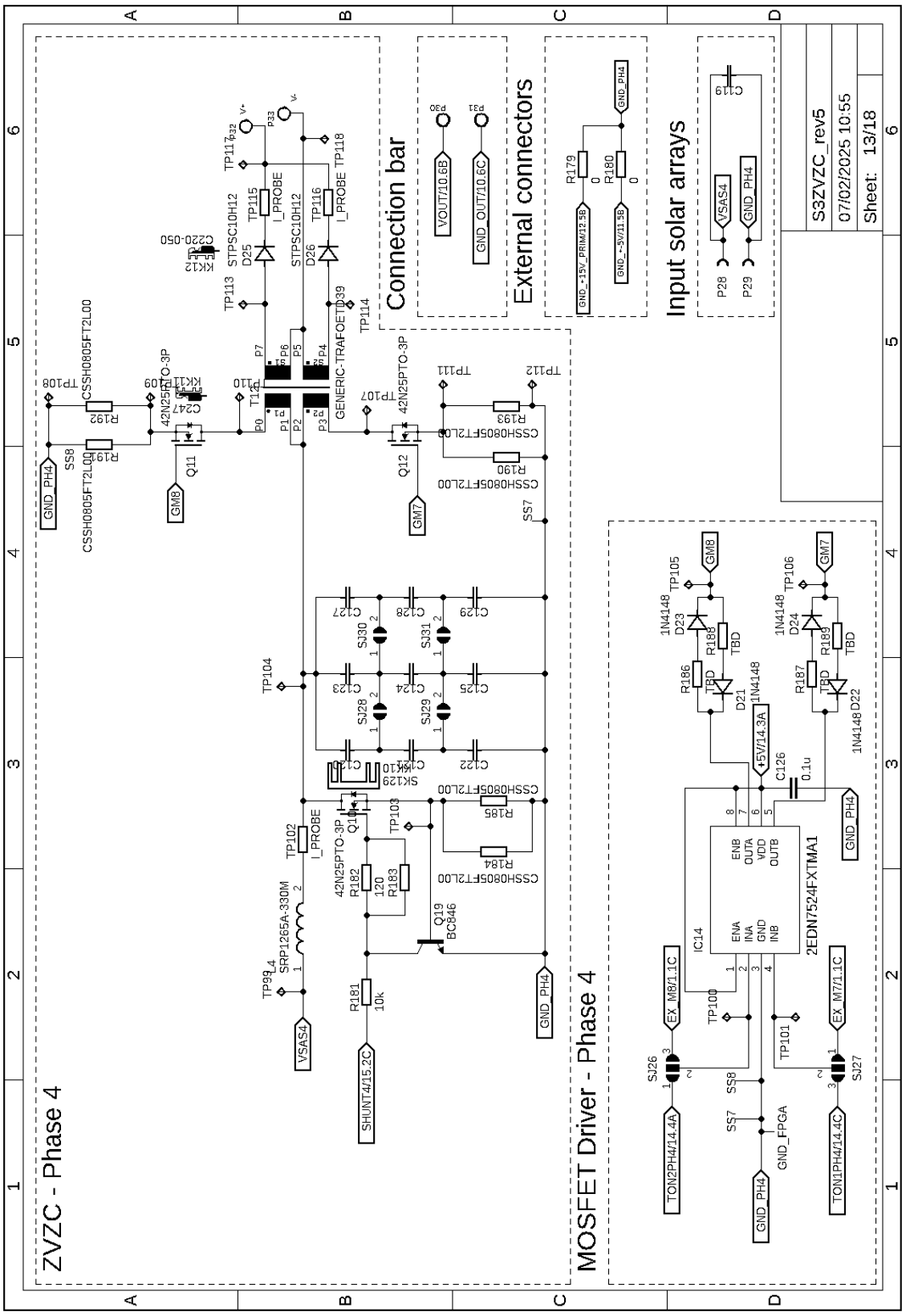

Figure 82. S3DCX prototype schematic – Power cell 4.

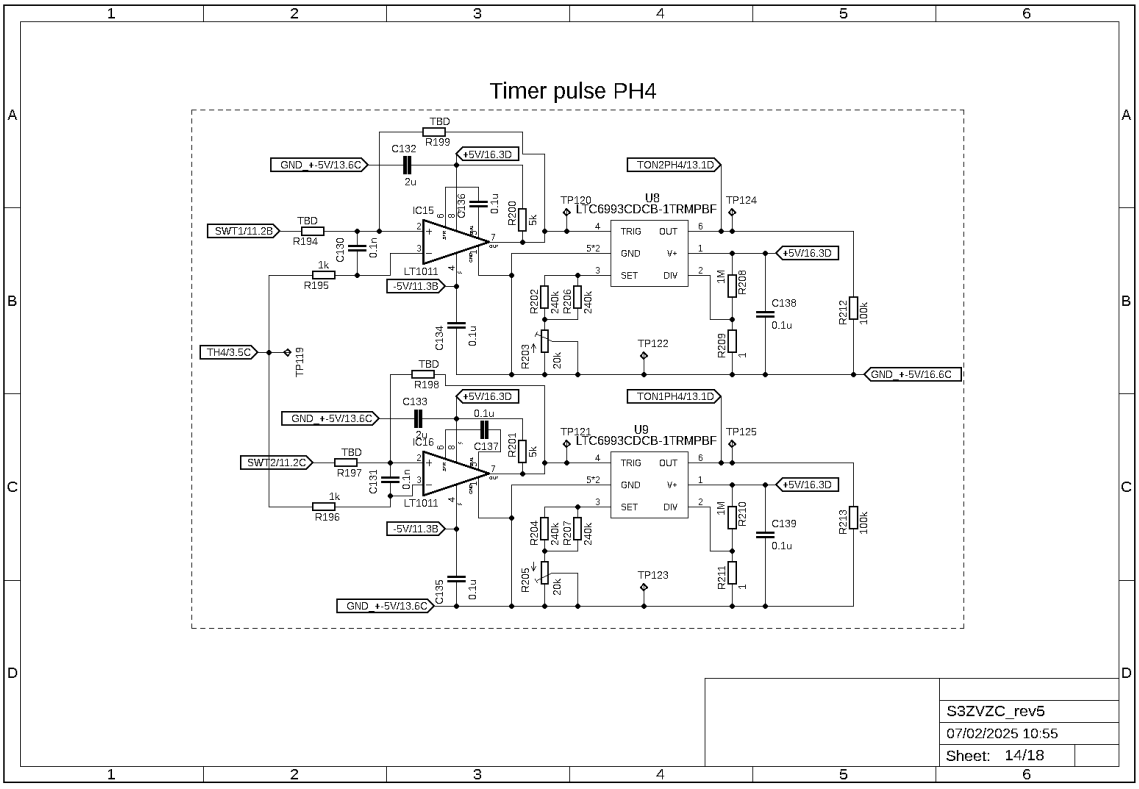

Figure 83. S3DCX prototype schematic – Timer pulse phase 4.

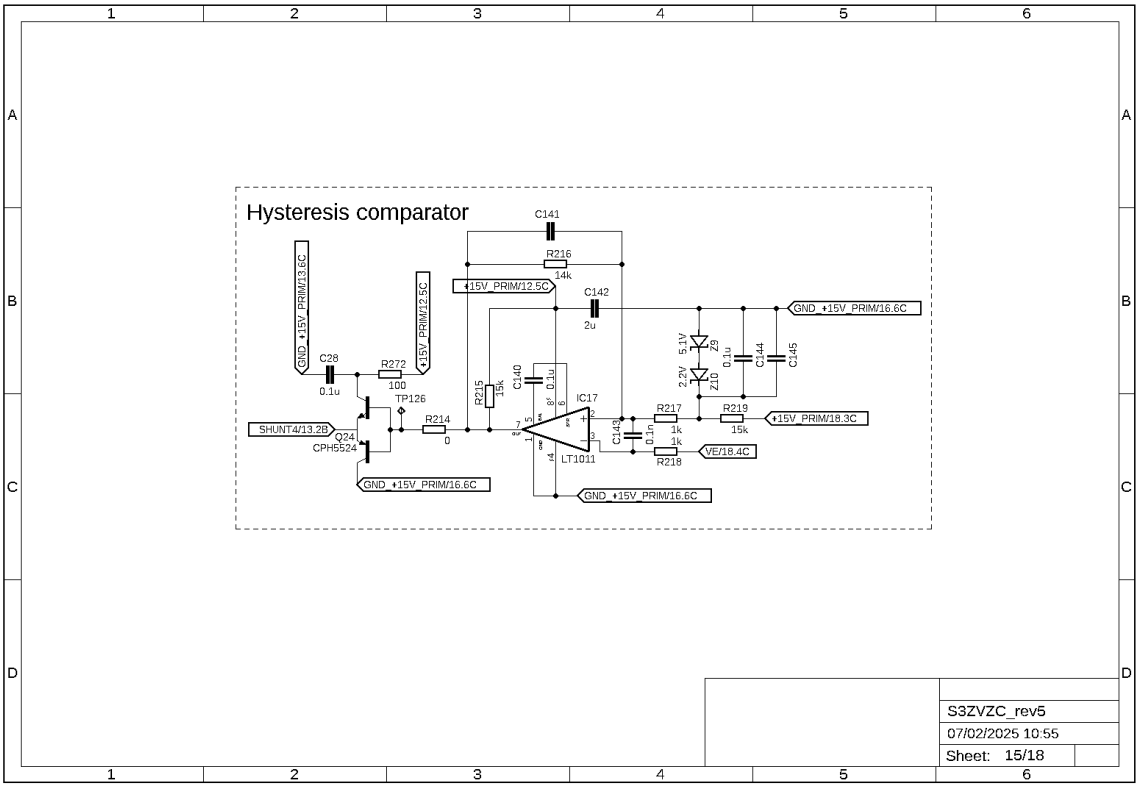

Figure 84. S3DCX prototype schematic – Hysteresis comparator phase 4.

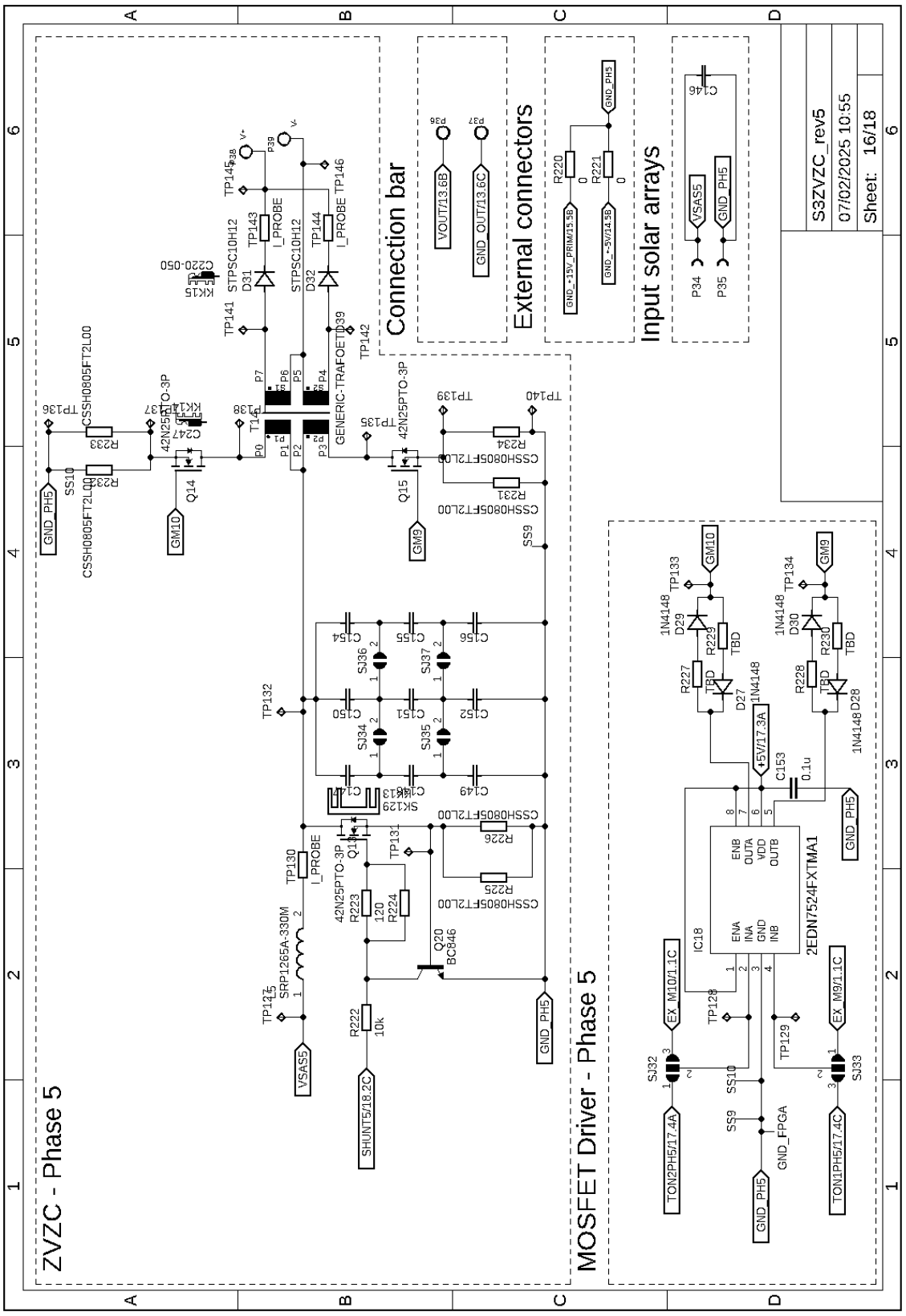

Figure 85. S3DCX prototype schematic – Power cell phase 5.

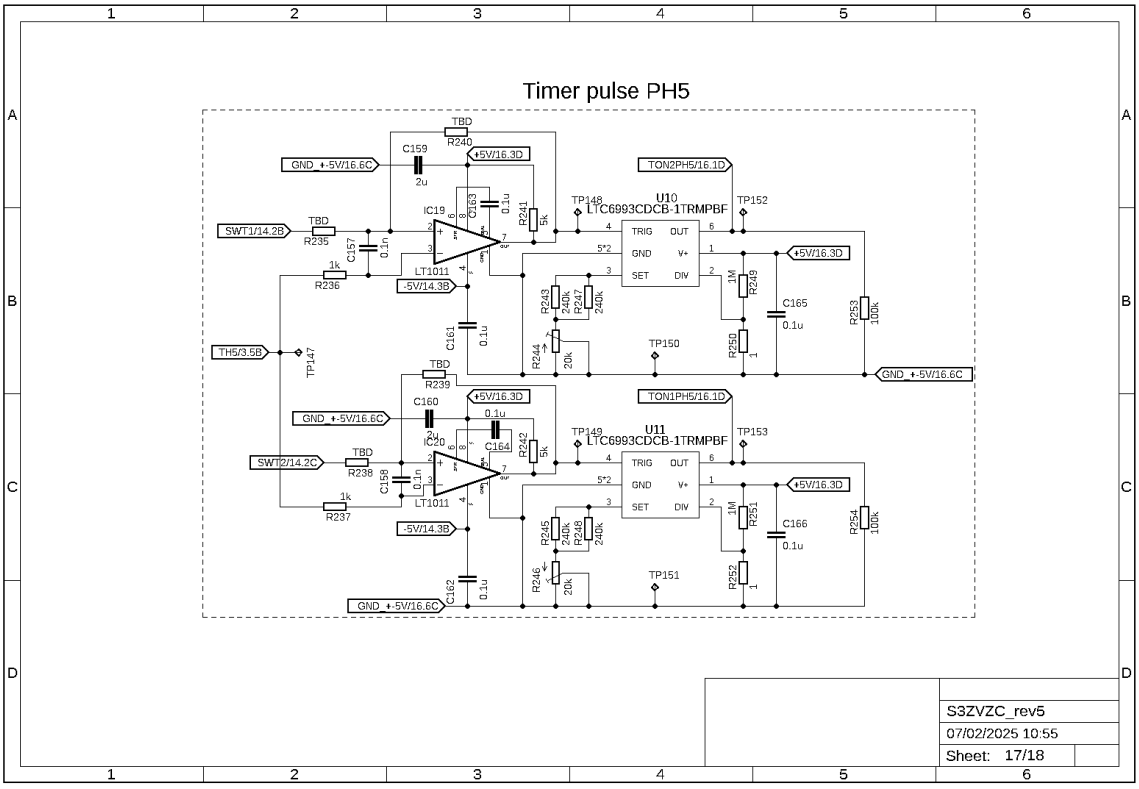

Figure 86. S3DCX prototype schematic – Timer pulse phase 5.

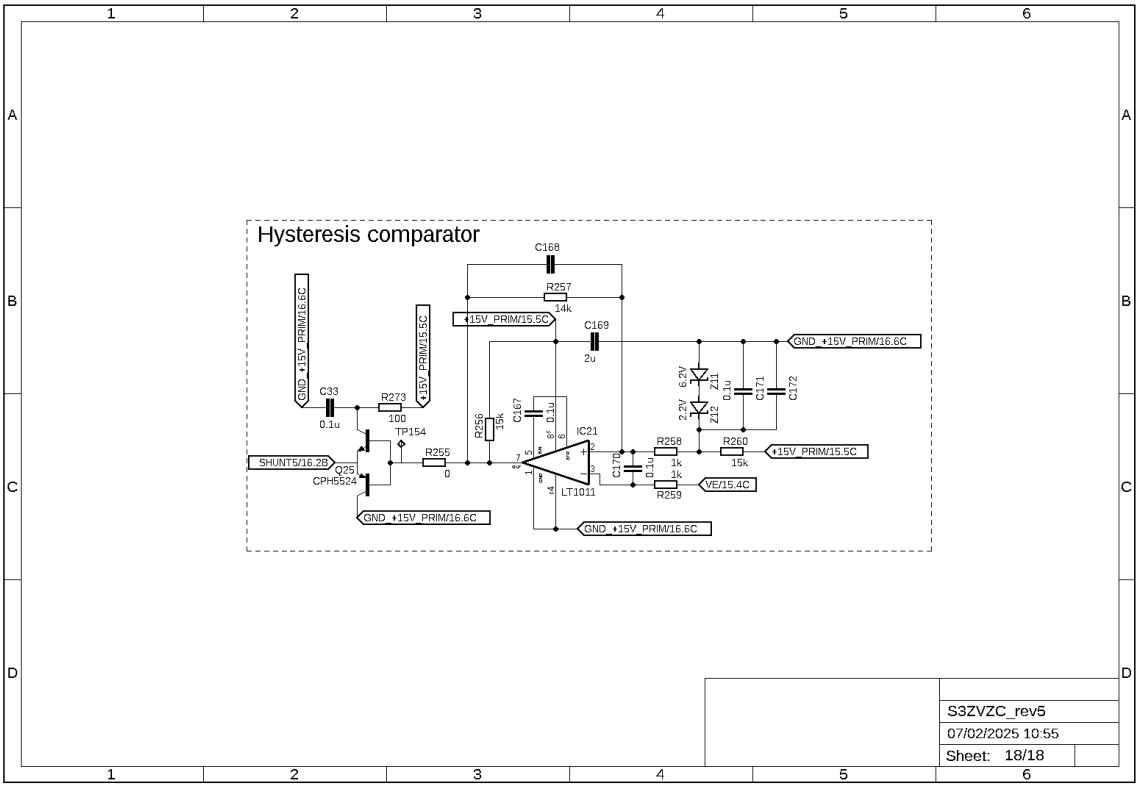

Figure 87. S3DCX prototype schematic – Hysteresis comparator phase 5.

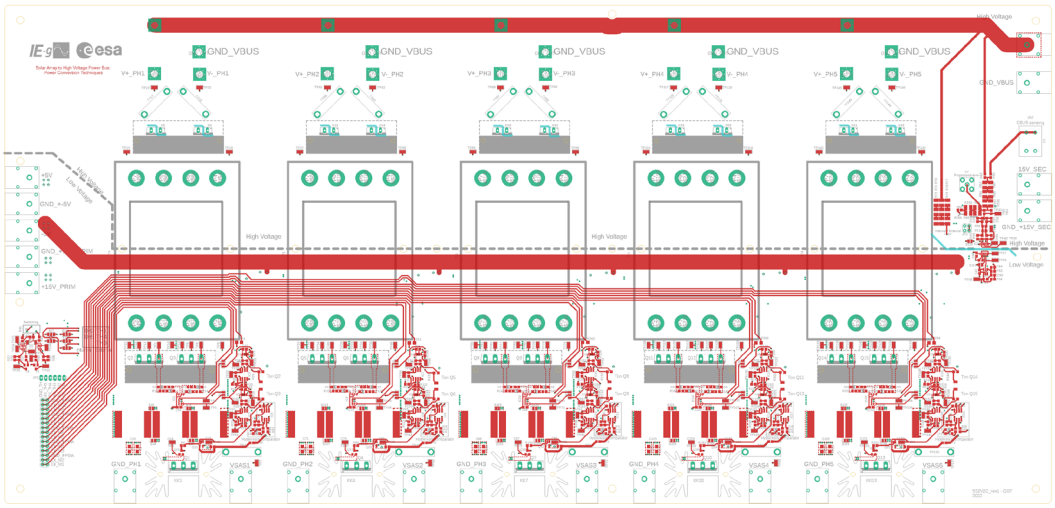

Figure 88. S3DCX board schematic – Top layer.

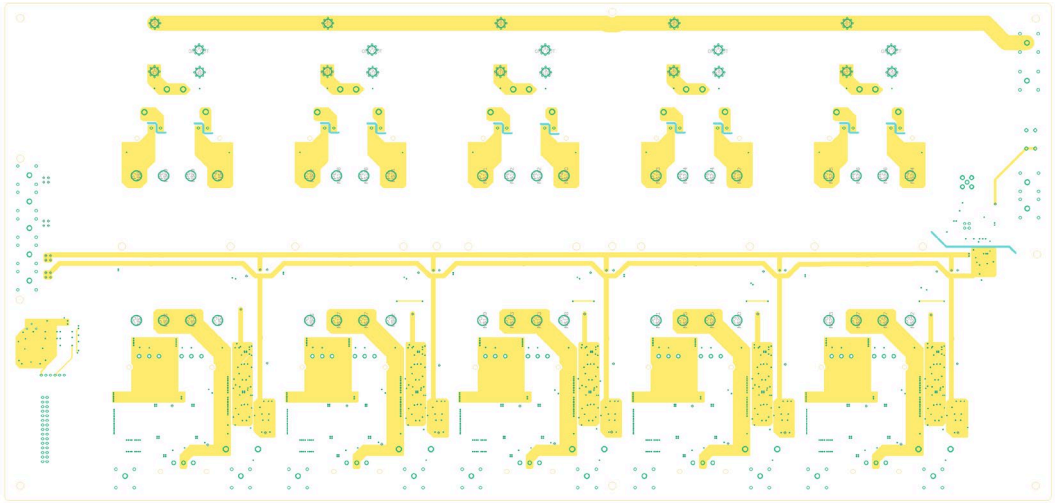

Figure 89. S3DCX board schematic – Second layer.

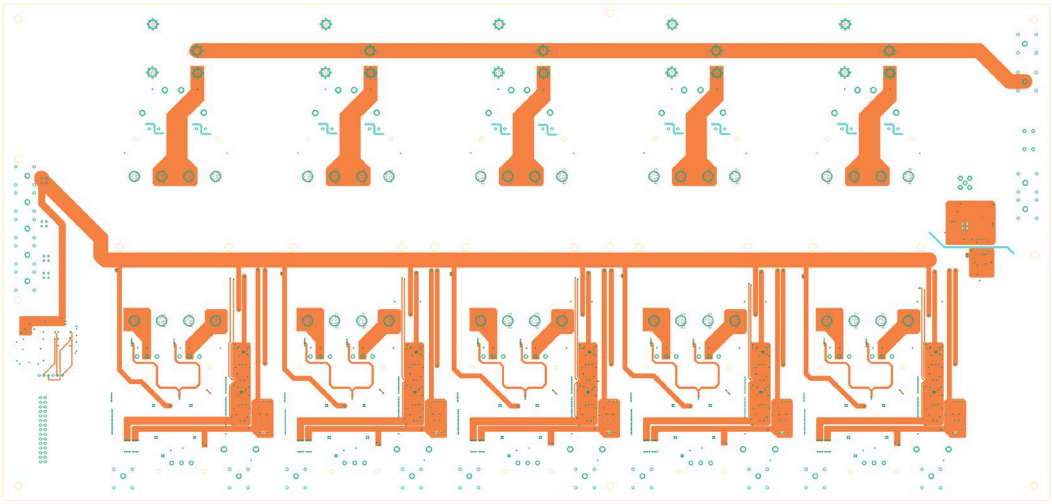

Figure 90. S3DCX board schematic – Third layer.

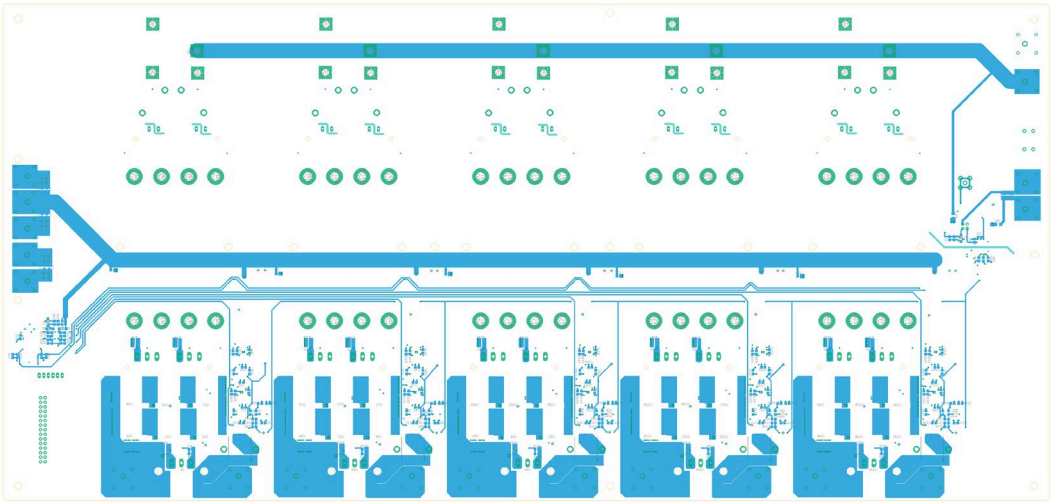

Figure 91. S3DCX board schematic – Bottom layer.

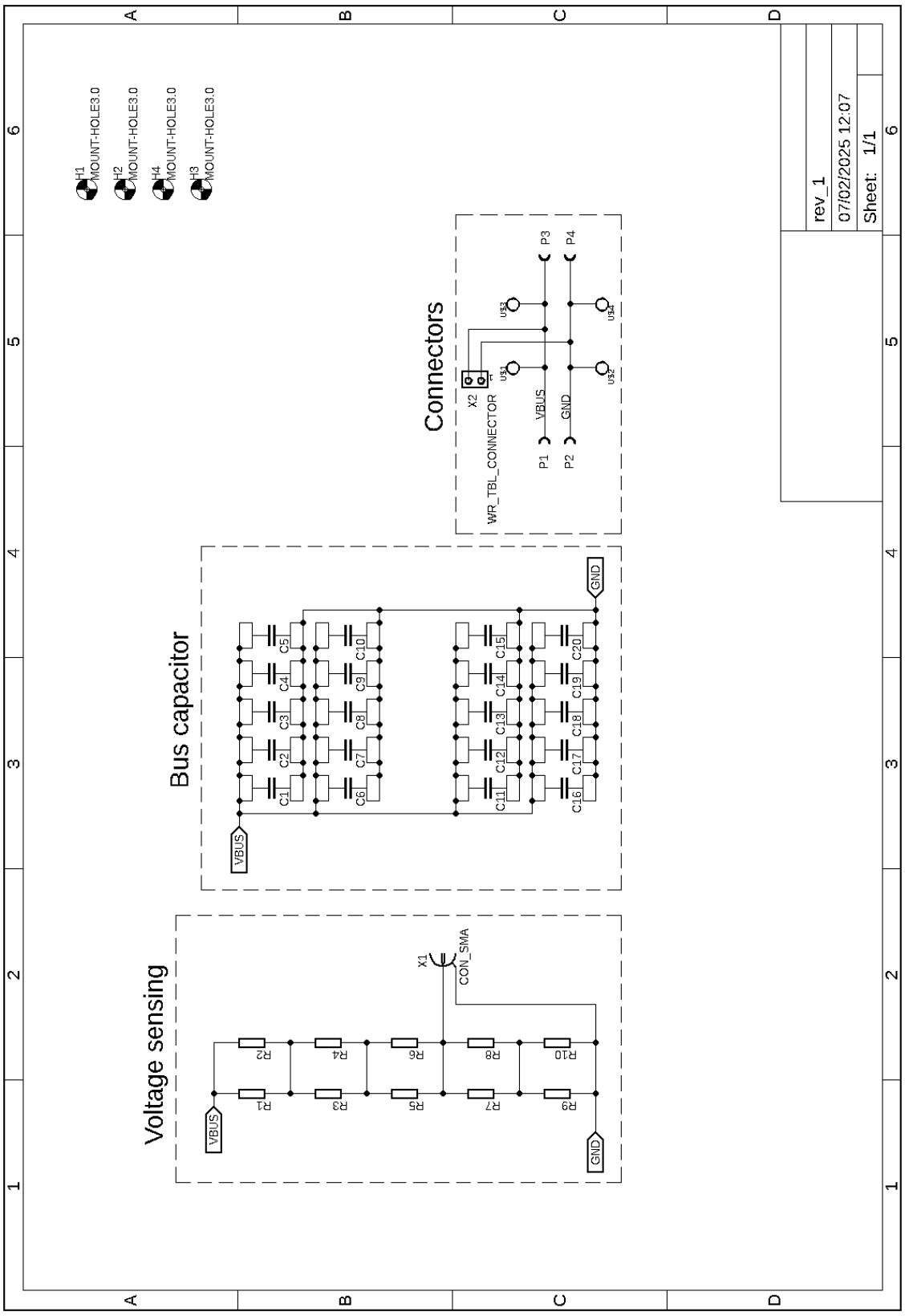

Figure 92. Bus capacitor schematic.

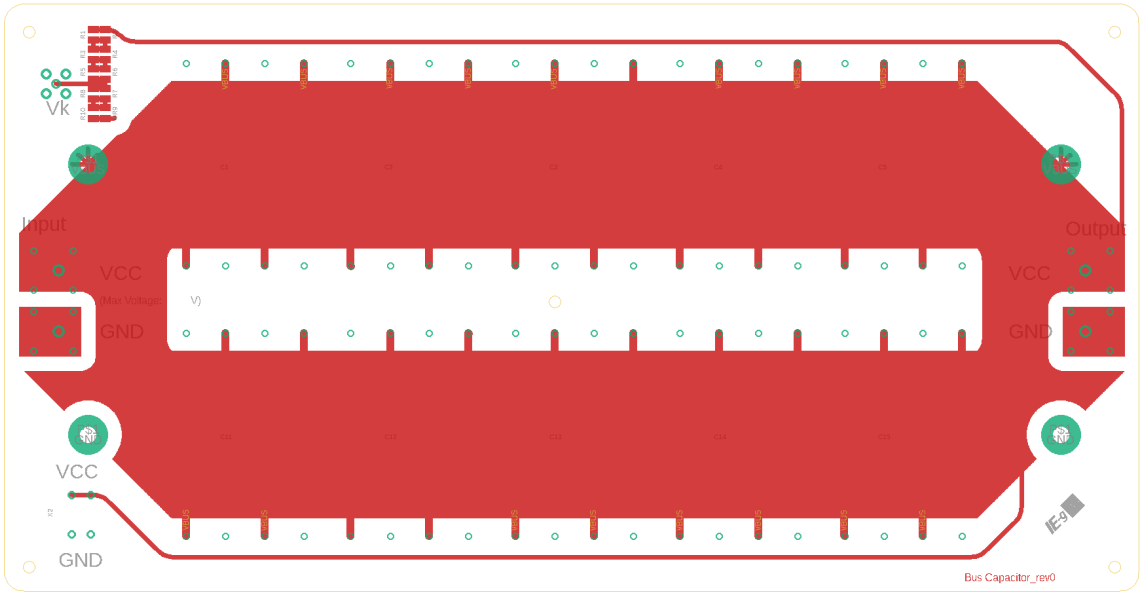

Figure 93. Bus capacitor board – Top layer.

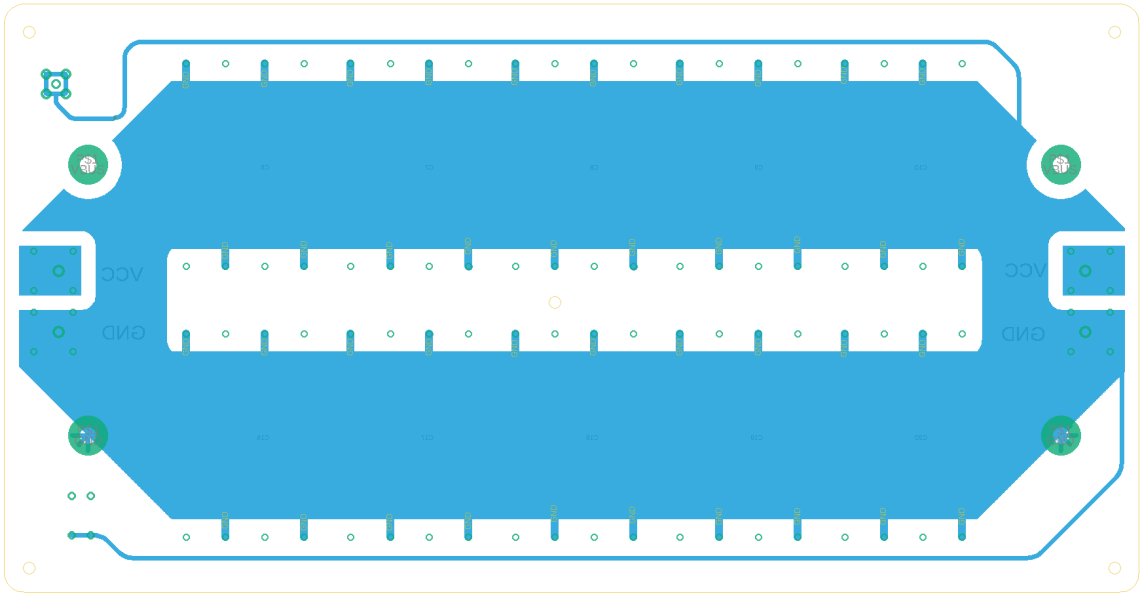

Figure 94. Bus capacitor board – Bottom layer.

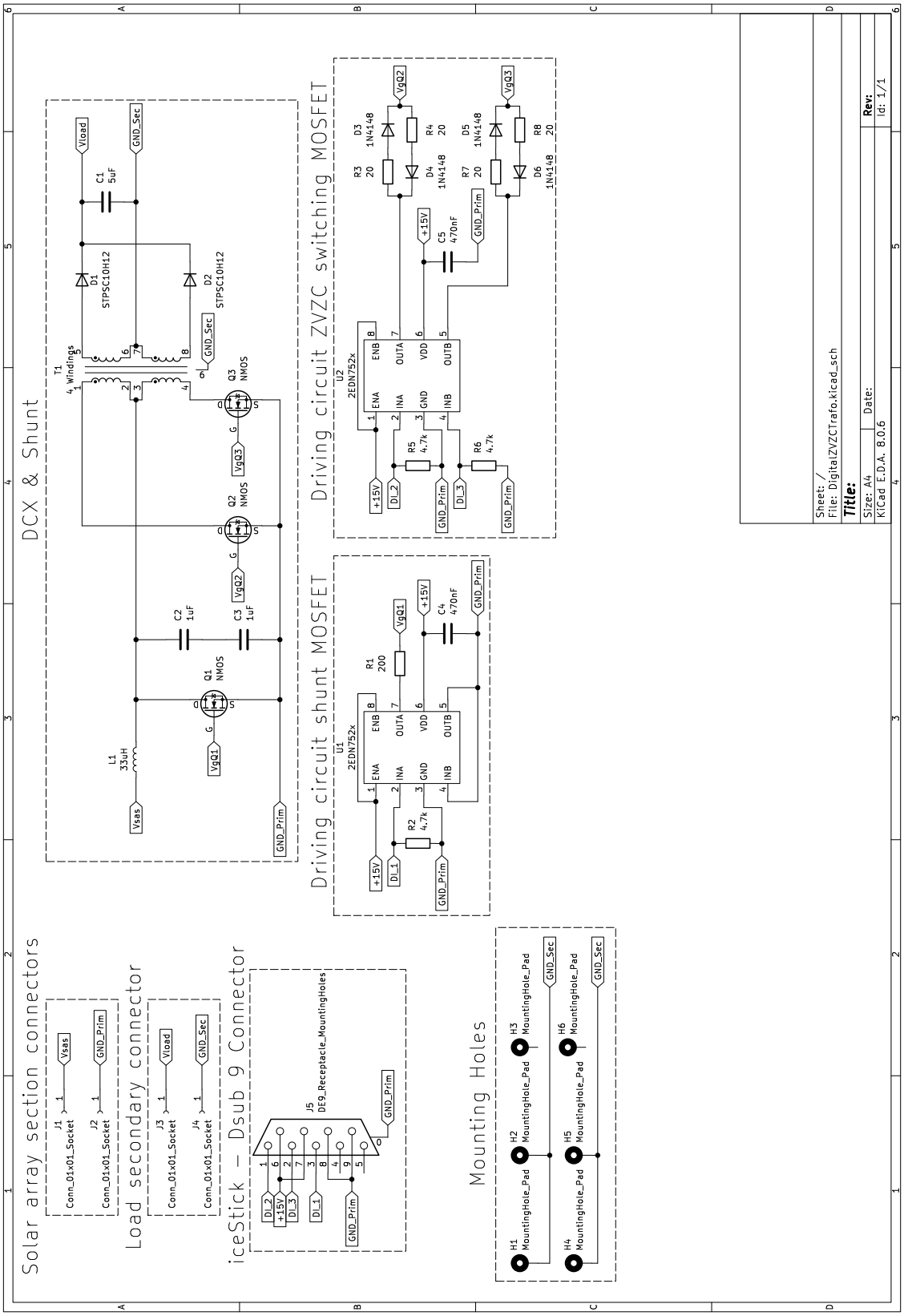

Figure 95. Power cell schematic for vacuum test.

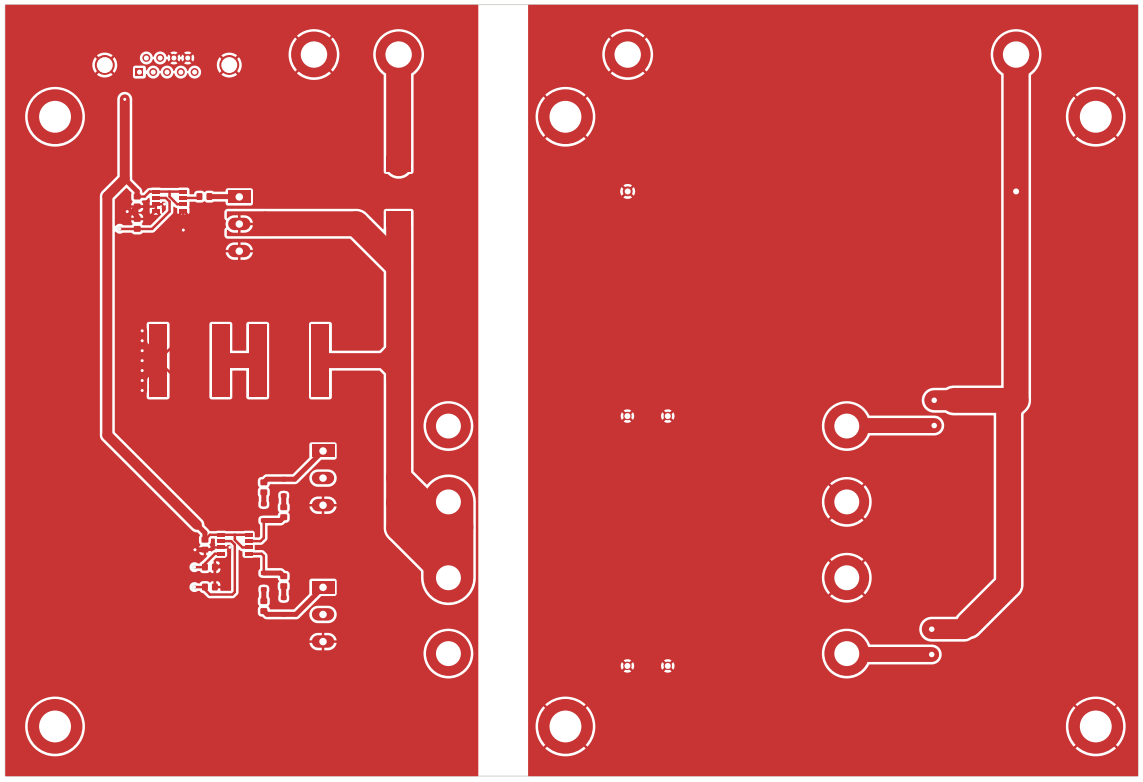

Figure 96. Power cell board for vacuum tests – Top layer.

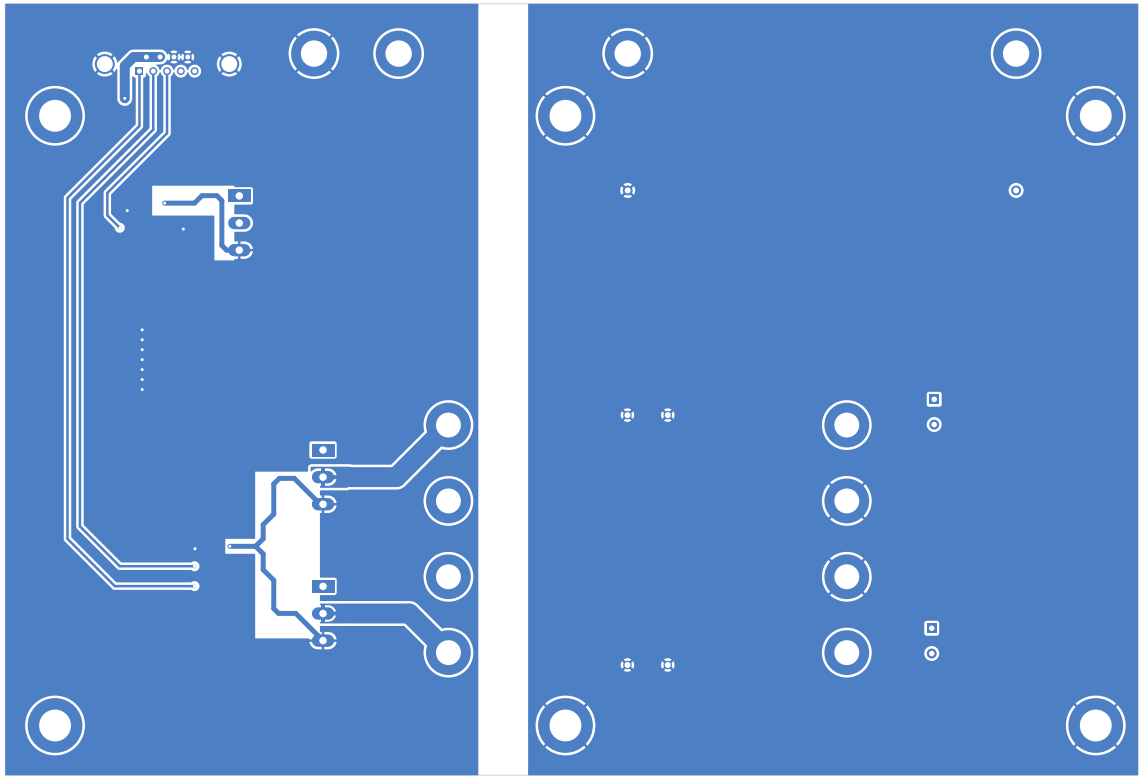

Figure 97. Power cell board for vacuum tests – Bottom layer.

Annex II

Description of experimental setup

A series of laboratory equipment have been utilised for the experimental validation of the concepts and prototypes presented within the present thesis. The following list provides a brief description of the main equipment used for the S3DCX validation in the SPES research laboratories, which are located at the Miguel Hernández University of Elche.

- **Solar array simulator Agilent E4351B:** The solar array simulator operates as a programmable power source that replicates the I-V curve of the solar panels. In this work, it has been employed as the main power source for validating the S3DCX.

- **Oscilloscope Tektronix DPO4034:** In order to capture voltage and current measurements and waveforms, a 4-channel oscilloscope is employed. This equipment has been extensively utilised throughout the thesis for the development and validation of prototypes.

- **Oscilloscope Tektronix MSO46:** In situations where the acquisition of data necessitates the utilization of more than four channels, the deployment of a 6-channel oscilloscope is used.

- **Bench power resistors:** In order to simulate the loads connected to the distribution bus, two benches of power resistors are used. These benches consist of five independent 470 Ω resistors (TE500B470RJ) and ten 100 Ω resistors (TE200B100RJ). The resistors are enclosed in a metallic box and connected externally with banana connectors.

- **Multimeter Fluke 8846A:** A high-precision multimeter was utilised to measure the winding resistance of the transformers, by employing a 4-wire measurement technique.

- **Vector network analyser OmicronLab Bode100:** The vector network analyser has been employed for the characterisation of electric components, including the DCX transformers and the bus capacitor.

- **Power analyser Yokogawa WT1800:** The equipment was employed to measure the power generation and power consumption with the objective of accurately obtaining the efficiency of each power cell.

- **Thermographic camera FLUKE Ti450:** In order to facilitate an understanding of the heat distribution, maximum temperature of the components, and overall power losses, the utilisation of a thermographic camera is required.

- **Digital control board SPCard:** An FPGA is used to command the control signals for switching between the resistive loads for the S3DCX prototype.

As shown in Figure 98, the most commonly employed experimental setup for evaluating and validating the S3DCX are presented. It should be noted that the solar array simulators and the bench power resistors are depicted outside the image.

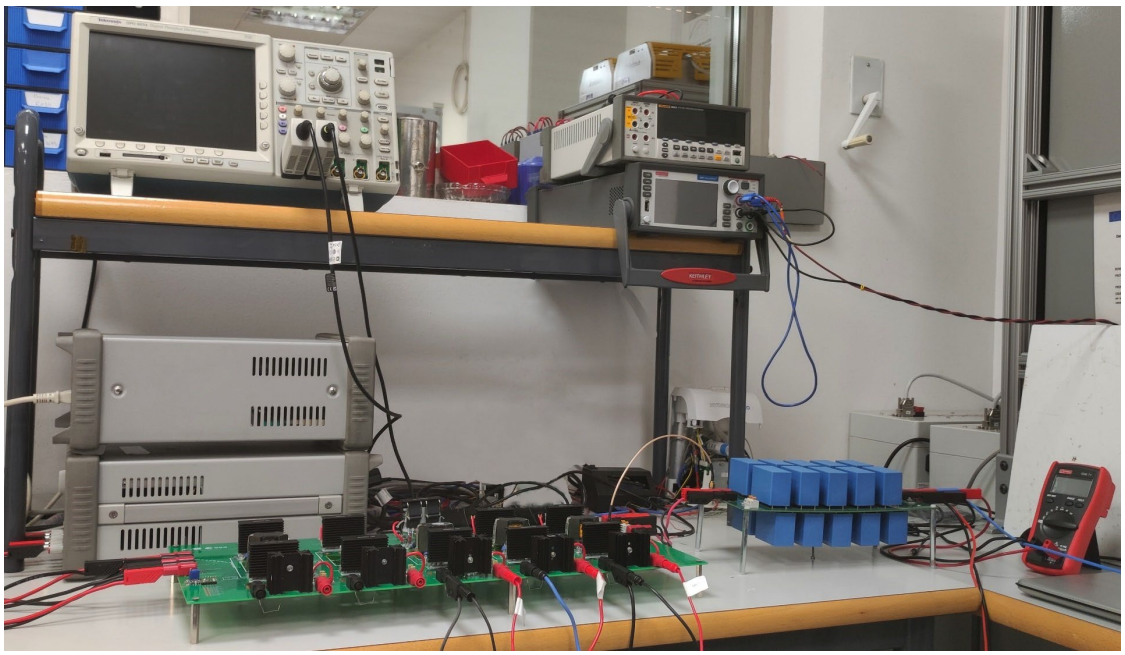

Figure 98. Picture of the experimental setup for the S3DCX prototype.

The study of the electric isolation of the transformers and S3DCX under ambient and vacuum conditions was conducted at the High voltage facilities of TEC-EP in ESTEC ESA. The main equipment used is listed and described below:

- **Non-destructive insulation tester JP 30A:** With the objective to measure the electrical isolation between the transformer windings without damaging the isolators. A 30 kV – 0,2 mA insulator tester has been used.

- **Solar array simulator Agilent E4360A:** A programmable solar array simulator is used as the power source for a single power cell during the testing and validation during the test in the vacuum chamber.

- **DC electronic load Chroma 63630-600-15:** For the purpose of simulating different resistive loads at the output of the power cell during the vacuum tests, a programmable electronic load is used.

- **High voltage vacuum chamber**: With the objective to simulate the ambient conditions of space and test the electric isolation of the power cell and transformer, a vacuum chamber capable of achieving pressures down to 10^{-4} mbar.

- **Pressure sensor Pfeiffer PKR 251:** In order to fully assess the high voltage effects during the partial pressure test, a pressure measurement inside the vacuum chamber is required. The sensor has a measuring range of $5 \cdot 10^{-9}$ to 1000 mbar with an accuracy of ±30 %.

The experimental setup used for the study of electric isolation and the validation of the power cell under vacuum conditions, is shown in Figure 99.

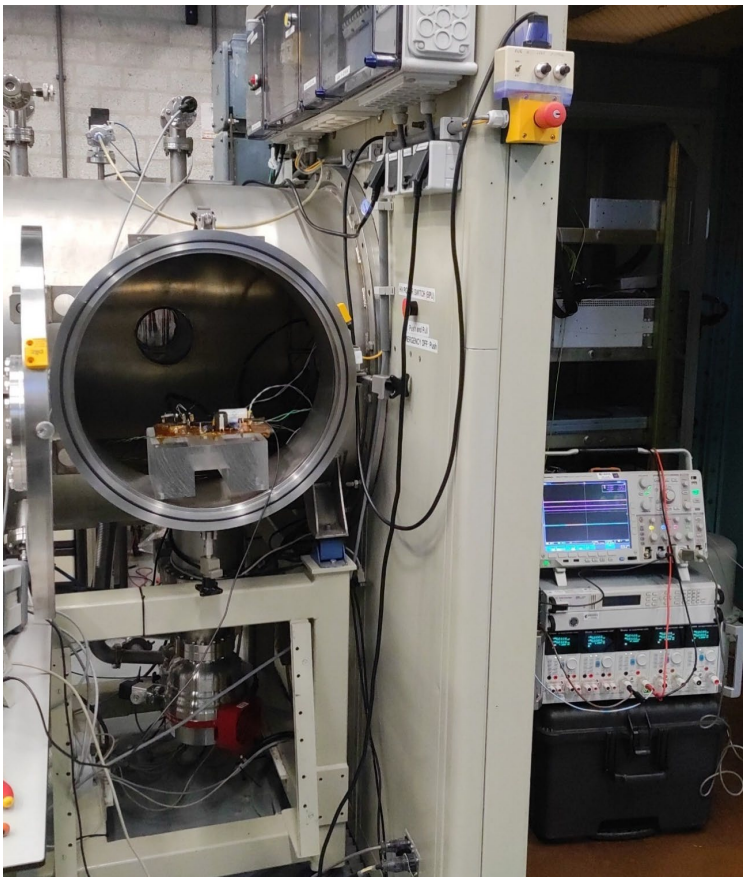

Figure 99. Picture of the experimental setup for the power cell under vacuum conditions.

Annex III

Software for S3DCX design methodology calculation

In this annex is presented the software, which was implemented in *Python,* used for the calculation of the S3DCX methodology proposed in Chapter 3.

The code for the S3DCX design methodology is presented.

```
import numpy as np
import matplotlib.pyplot as plt
import matplotlib.ticker as ticker
import matplotlib.patches as patches
import TransfomerDesign as trd
from scipy.optimize import fsolve

#----S3DCX Specifications---#

Vi = 100            #Input voltage of the converter
Ii = 4              #Input current of the converter
Vo = 300            #Output voltage of the converter
N = Vo/Vi           #Transformation ratio
Pi = Vi*Ii          #Input power

#--------------------------------
#----Components specifications---
# *All units are in *

ron = 84*10**-3     #MOSFET internal resistance
Cds = 350*10**-12   #MOSFET drain-source capacitance
ParalMOS = 1        #Number of MOSFETs in parallel
pCr = 50*10**-4     #Dissipation factor of the resonant capacitor
Vf = 0.9            #Forward voltage rectifier diode at output current
(Ii/N)
Cj = 100*10**-12    #Junction capacitance of rectifier diode
SerieDio = 1        #Number of Diodes in series
Ctr = 300*10**-12   #Transformer capacitance - Estimation
Lh = 33*10**-6      #Harness inductance

#--------------------------------
#----Range of possible Im----

Im1 = Ii*0.01                               #Minimum Magnetizing Current
Im2 = Ii*0.25                               #Maximum Magnetizing Current
Im = np.array(list(np.arange(Im1,Im2,0.025))) #Array of possibles Im

#--------------------------------
#----Timing aproximation of ton and tgap----

Ceq = Cds+Ctr+Cj*N**2               #Equivalent parasitic capacitance
Window_D = 0.754                    #Switching duty cycle
tgap_st = (4*Vi*Ceq)/Im             #Estimation of tgap
ton_st = tgap_st*Window_D/(1-Window_D)  #Estimation of ton
fc_st = 1/(2*(ton_st+tgap_st))      #Array of switching frequency
#Relationship between ton and tgap
kT_st = (tgap_st**2)/(ton_st+tgap_st)
#Estimation resonance frequency during ton
wr_st = 2*np.pi/(ton_st+tgap_st)
Lmmax = (Vi*ton_st)/(2*Im)   #Maximum allowable Magnetizing inductance

#--------------------------------
#----First estimation of the resonance frequency----

def f(variables,i): #Function to calculate the angular resonance
frequency
    wr_st = variables
```

```
    y = np.cos(wr_st*ton_st[i])-
wr_st*0.5*tgap_st[i]*np.sin(wr_st*ton_st[i])-1
    return y

i = 0
wr = np.zeros(np.size(wr_st))
while i < np.size(wr_st):
    wr[i] = fsolve(f, wr_st[i], i)  #Calculation by numerical methods
    i = i + 1
fr = wr/(2*np.pi)                   #Resonant frequency for each Tgap
#Phase of the resonance
phi = np.arctan((wr*(tgap_st**2))/(ton_st+tgap_st))

#---------------------------------
#----Obtaing a list of transformers based on a database----
wff = 0.3            #Winding factor
I_density = 3*10**6  #Maximum current density
#Primary current RMS
Iprms =
Ii*np.sqrt((ton_st+ton_st/(2*np.power(np.cos(phi),2))+(3*np.tan(phi))/
(wr))/(ton_st+tgap_st))

rawTrafo = rawTrafo = [dict() for x in range(np.size(Im))]

i = 0
while i < np.size(Im):
    rawTrafo[i] =
trd.TransformerComparator(Lmmax[i],Vi,ton_st[i],N,wff,fc_st[i],Iprms[i
],I_density)
    i = i + 1

#---------------------------------
#----Calculate FoM for each transformer and selection of best option--
--

i = 0
j = 0
k = 0
varFom = 10**20

refFom = np.zeros(np.size(Im))
indexMaterial = np.zeros(np.size(Im))
indexCore = np.zeros(np.size(Im))

while i < np.size(Im): #Tgap --> Material --> Core
    while j < len(rawTrafo[i]):
        while k < len(rawTrafo[i][j]):
            fom = rawTrafo[i][j]['Total_losses [W]'][k] *
rawTrafo[i][j]['Weight [kg]'][k] #Transformer's figure of merits
dependent of mass and losses
            if (fom < varFom) and (fom != 0): #Update minimum FoM and
index selection
                varFom = fom
                refFom[i] = varFom
                indexMaterial[i] = j
                indexCore[i] = k
            k = k + 1
        j = j + 1
        k = 0
```

```
    i = i + 1
    j = 0
    varFom = 10**6

n1 = np.zeros(np.size(Im))              #n1 initialization
n2 = np.zeros(np.size(Im))              #n2 initialization
Lm = np.zeros(np.size(Im))              #Lm initialization
Llk = np.zeros(np.size(Im))             #Llk initialization
Ptr = np.zeros(np.size(Im))             #Ptr initialization
Wt = np.zeros(np.size(Im))              #Wt initialization
Dn1 = np.zeros(np.size(Im))
Dn2 = np.zeros(np.size(Im))

i = 0
#Filter non valid Tgap and select parameters of the transformer
while i < np.size(Im):
    if rawTrafo[i][indexMaterial[i]]['N1'][indexCore[i]] > 0:
        Lm[i] =
rawTrafo[i][indexMaterial[i]]['Lm_teórica[uH]'][indexCore[i]]/(10**6)
        Llk[i] = 427*10**-9     #Obtained with FEMM simulation for a
particular case
        n1[i] = rawTrafo[i][indexMaterial[i]]['N1'][indexCore[i]]
        n2[i] = rawTrafo[i][indexMaterial[i]]['N2'][indexCore[i]]
        Ptr[i] = rawTrafo[i][indexMaterial[i]]['Total_losses
[W]'][indexCore[i]]
        Wt[i] = rawTrafo[i][indexMaterial[i]]['Weight
[kg]'][indexCore[i]]
        Dn1[i] = rawTrafo[i][indexMaterial[i]]['Dprim
[mm]'][indexCore[i]]
        Dn2[i] = rawTrafo[i][indexMaterial[i]]['Dsec
[mm]'][indexCore[i]]
    else:
        Lm[i] = np.nan
        Llk[i] = np.nan
        n1[i] = np.nan
        n2[i] = np.nan
        Ptr[i] = np.nan
        Wt[i] = np.nan
        Dn1[i] = np.nan
        Dn2[i] = np.nan
    i = i + 1

#--------------------------------
#----Calculate ton and tgap values and update timing parameters----

def TonTgap(variables, i):
    (ton,tgap) = variables
    tonX = ton
    tgapY = tgap
    theta = np.arctan(-np.sqrt(2)/(wgap[i]*tonX))
    eqn_1 = np.sin(wgap[i]*tgapY+theta)-np.sin(theta)-
(8*Lm[i]*wgap[i]*Ceq*np.cos(theta))/(tonX)
    eqn_2 = np.cos(wr[i]*(tonX))-wr[i]*(tgapY)/2*np.sin(wr[i]*(tonX))-
1
    return [eqn_1,eqn_2]

Im_st = Vi*ton_st/(2*Lm)
tgap_2st = 2*Vi*Ceq/Im_st
wgap = 1/np.sqrt(2*Lm*Ceq)
```

```
i = 0
Ton = np.zeros(np.size(ton_st))
Tgap = np.zeros(np.size(tgap_st))
#Ton and Tgap are obtained by numerical methods solving the equation
system
while i < np.size(tgap_st):
    [Ton[i], Tgap[i]] = fsolve(TonTgap, (ton_st[i],tgap_2st[i]), i)
    i = i + 1

ImPlot = 0.5*Vi*Ton/Lm      #Magnetizin current updated
#The array is sorted given that its possible that the values Im are
not correctly in position after previous calculations
ind = np.argsort(ImPlot)
ImPlot = ImPlot[ind]
Ton = Ton[ind]
Lm = Lm[ind]
Llk = Llk[ind]
n1 = n1[ind]
n2 = n2[ind]
Ptr = Ptr[ind]
Wt = Wt[ind]
wgap = wgap[ind]
Dn1 = Dn1[ind]
Dn2 = Dn2[ind]
indexMaterial = indexMaterial[ind]
indexCore = indexCore[ind]
rawTrafo = [rawTrafo[i] for i in ind]

#Angle tecta of the resonance
tecta = np.arctan(-np.sqrt(2)/(wgap*Ton))
#Phase of the resonance
phi = np.arctan((wr*(Tgap**2))/(Ton+Tgap))
fc = 1/(2*(Ton+Tgap))                  #Array of switching frequency
kT = (Tgap**2)/(Ton+Tgap)              #Relation between Ton and Tgap
fr = wr/(2*np.pi)                      #Resonant frequency for each Tgap
Cr = (Llk+Lh)/(Llk*Lh*wr**2)           #Resonant capacitor

#--------------------------------
#----Power losses calculations----

Vpk = (2*Ii)/(wr*Cr*np.cos(phi))       #Peak to peak Vds ripple
#MOSFET Voltage at the instant of switching at Ton
von = (Iprms/ParalMOS*Tgap**2)/(Cr*(Ton+Tgap))
#Primary current RMS
Iprms =
Ii*np.sqrt((Ton+Ton/(2*np.power(np.cos(phi),2))+(3*np.tan(phi))/(wr))/
(Ton+Tgap))
#Current capacitor RMS
Icrms = Ii*np.sqrt(1/(Ton+Tgap)*(Ton/(2*np.cos(phi)**2)+Tgap-
np.tan(phi)/wr))
#Resonant capacitor power losses
Pcr = Icrms**2*pCr/(wr*Cr)
#Conduction power losses per MOSFET
PcondMOS = (Iprms/ParalMOS)**2*ron
#Total conduction power losses
Pcond = PcondMOS*ParalMOS
#Switching power losses per MOSFET
PswMOS = Cds*von**2*fc
```

```
#Total switching power losses
Psw = PswMOS*ParalMOS
#Diode rectifier power losses per MOSFET
PdrDio = (Vf*Iprms)/((Ton+Tgap)*N)*(Ton+(2*np.tan(phi)/wr))
#Diode rectifier power losses
Pdr = PdrDio*SerieDio
#Total power losses
Pt = Pcr + Pcond + Psw + Pdr + Ptr

#---------------------------------
#----Plot of efficiencies respect Im----

Im_norm = ImPlot/Ii
Eff_theor = (Pi-Pt)/Pi*100
FoM_theor = Wt*Eff_theor

Max_Ind = list(Eff_theor).index(np.nanmax(Eff_theor))
Min_FoM = list(FoM_theor).index(np.nanmin(FoM_theor))
Im_max = Im_norm[Max_Ind]

for i in range(np.size(FoM_theor)):
    if FoM_theor[i] <= 0:
        FoM_theor[i] = 10**6

Ton_figure = Ton
Tgap_figure = Tgap
Ton_figure[0:Max_Ind] = [-1] * Max_Ind
Tgap_figure[0:Max_Ind] = [-1] * Max_Ind

Area_prim = np.pi*(Dn1/2)**2
Area_sec = np.pi*((Dn2/2)**2)
J1_density = Iprms/Area_prim
J2_density = Iprms/(Area_sec*N)

minX = 0.05
maxX = 0.20
minY1 = 94
maxY1 = 98.5
minY2 = 0
maxY2 = 9

rectJmax = patches.Rectangle((minX,minY1),Im_norm[Max_Ind]-minX,maxY1-
minY1, alpha = 0.15, color = 'C1')

indexA = Max_Ind
indexB = 18
indexC = 23
#Coordinates [[x0,x1],[y0,y1]]
lineA = [[Im_norm[indexA],Im_norm[indexA]],[minY1,maxY1]]
lineB = [[Im_norm[indexB],Im_norm[indexB]],[minY1,maxY1]]
lineC = [[Im_norm[indexC],Im_norm[indexC]],[minY1,maxY1]]

fig, ax1 = plt.subplots()
#Efficiency data
ax1.plot(Im_norm,Eff_theor,label='Efficiency', color = 'C3', marker =
'.', linewidth = 2, markersize = 10)
#Line selection
ax1.plot(lineA[0],lineA[1], color = 'k',linestyle='dashed', linewidth
= 1.5)
```

```
ax1.plot(lineB[0],lineB[1], color = 'k',linestyle='dashed', linewidth
= 1.5)
ax1.plot(lineC[0],lineC[1], color = 'k',linestyle='dashed', linewidth
= 1.5)
#Text points
ax1.text(Im_norm[indexA]*0.942,Eff_theor[indexA]*1.001,'A)', fontsize
= 24)
ax1.text(Im_norm[indexB]*0.965,Eff_theor[indexB]*0.998,'B)', fontsize
= 24)
ax1.text(Im_norm[indexC]*0.97,Eff_theor[indexC]*1.002,'C)', fontsize =
24)
#Text loss text regions
ax1.text(0.0625,97.3,'Exceeded\n$\mathrm{J_{max}}$', fontsize = 26, ha
= 'center', weight = 'bold')
#Patches
ax1.add_patch(rectJmax)

ax1.set_ylim([minY1,maxY1])
ax1.set_xlim([minX,maxX])

ax1.set_ylabel('EFficiency [%]',fontsize = 24)
ax1.set_xlabel('Normalized magnetizing current
'+'$(\mathrm{I_m/I_{SAS}})$',fontsize = 24)

ax1.xaxis.set_major_locator(ticker.MultipleLocator(0.05))
ax1.xaxis.set_minor_locator(ticker.MultipleLocator(0.025))
ax1.yaxis.set_major_locator(ticker.MultipleLocator(1))
ax1.yaxis.set_minor_locator(ticker.MultipleLocator(0.5))

ax2 = ax1.twinx()
ax2.plot(Im_norm,Ton_figure*10**6,label='$\mathrm{t_{on}}$',linestyle=
'dashed',color='g',marker='.', markersize = 10)
ax2.plot(Im_norm,Tgap_figure*10**6,label='$\mathrm{t_{gap}}$',linestyl
e='dashed',color='C0',marker='.', markersize = 10)

ax2.set_ylim([minY2,maxY2])

ax2.set_ylabel('DCX timing '+' $[\mathrm{\mu s}]$',fontsize = 24)

ax2.yaxis.set_major_locator(ticker.MultipleLocator(2))
ax2.yaxis.set_minor_locator(ticker.MultipleLocator(1))

ax1.tick_params(axis = 'x', labelsize = 24, pad = 10, length = 6)
ax1.tick_params(axis = 'y', labelsize = 24)
ax2.tick_params(axis = 'y', labelsize = 24)

ax1.grid(linestyle=':', which ='both', linewidth = 1.5)

fig.legend(fontsize = 24, loc = 'upper center',
bbox_to_anchor=(0.5,0.98),ncol = 4)

#---------------------------------
#----Selection of optimum DCX design----

CompleteFoM = Pt * Wt
PminInd = list(CompleteFoM).index(np.nanmin(CompleteFoM))
Pmin = Pt[PminInd]
OptTgap = Tgap[PminInd]      #Optimum Tgap
Optwr = wr[PminInd]          #Optimum resonant frequency
```

```
OptCr = Cr[PminInd]          #Resonant capacitor for optimum frequency
OptIprms = Iprms[PminInd]    #Current RMS for the optimum point
OptTon = Ton[PminInd]
#Switching frequency at optimum frequency
Optfc = 1/(2*(OptTon+OptTgap))
#Duty cycle at optimum switching frequency
OptD = OptTon/(2*(OptTon+OptTgap))

#Peak current during Ton at swith MOSFET
Ipk = Ii*(1+1/np.cos(phi[PminInd]))
#Maximum ripple Vds at swith MOSFET
optVmax = Vi + OptIprms/(Optwr*OptCr*np.cos(phi[PminInd]))
#Minimum ripplpe Vds at switch MOSFET
optVmin = Vi - OptIprms/(Optwr*OptCr*np.cos(phi[PminInd]))
optVpk = optVmax-optVmin        #Peak to peak Vds at switch MOSFET
Im = 0.5*Vi*OptTon/Lm[PminInd]  #Maximum magnetizing current

tperiod = 2*(OptTon+OptTgap)
tdelay = OptTon+OptTgap

print("------BREAKDOWN OF THE LOSSES------")
print("Minimum total losses Pmin:",round(Pmin,4),'W')
print("Resonant capacitor power losses:",round(Pcr[PminInd],4),'W')
print("Conduction power losses:",round(Pcond[PminInd],4),'W')
print("Switching power losses:",round(Psw[PminInd]*10**3,4),'mW')
print("Diode rectifier power losses:",round(Pdr[PminInd],4),'W')
print("Transformer power losses:",round(Ptr[PminInd],4),'W')
print("\n------TIME PARAMETERS------")
print("Ton =", round(OptTon*(10**6),4), "us;", "Tgap =",
round(OptTgap*(10**6),4), "us")
print("Switching frequency fc:",round(Optfc/10**3,4),"kHz","Duty cycle
D:",round(OptD,4))
#Parameters for LTSPICE
print("PULSE(0 15 0 1n 1n " + str(round(OptTon*10**6,2)) + "u " +
str(round(tperiod*10**6,2)) + "u)")
print("PULSE(0 15 " + str(round(tdelay*10**6,2)) + "u 1n 1n " +
str(round(OptTon*10**6,2)) + "u " + str(round(tperiod*10**6,2)) +
"u)")
print("\n------TRANSFORMER PARAMETERS------")
print("Primary turns n1:",n1[PminInd],"Secondary turns
n2:",n2[PminInd])
print("Maximum Magnetizing inductance
Lmmax:",round(Lmmax[PminInd]*10**6,4),'uH')
print("Magnetizing inductance
Lm:",round(Lm[PminInd]*(10**6),4),'uH;',"Magnitizing current
Im:",round(Im,4),'A')
print("Leakeage inductance Llk:",round(Llk[PminInd]*10**9,4),'nF')
display(rawTrafo[PminInd][indexMaterial[PminInd]].loc[[indexCore[PminI
nd]]])
print("------RESONANCE CHARACTERISTICS------")
print("Resonance frequency fc:",
round((Optwr/10**3)/(2*np.pi),4),'kHz')
print("Resonance capacitance Cr:", round(OptCr*10**6,4),'uF')
print("Current capacitor RMS:", round(Icrms[PminInd],4), 'A')
print("Peak current Ipk:", round(Ipk,4),'A')
print("Primary rms current Iprms:", round(OptIprms,4),'A')
print("Maximum ripple voltage Vmax:", round(optVmax,4),'V')
print("Minimum riple voltage Vmin:", round(optVmin,4),'V')
print("Peak to peak ripple voltage Vpk:", round(optVpk,4),'V')
```

```
print("Equivalent parasitic capacitance Ceq:", round(Ceq*10**12,4),
'pF')

IcMax = 8               #Maximum current per capacitor
Cn = 1*10**-6           #Value of single capacitor in the matrix
#String of capacitors in parallel.
Ncp = np.ceil(Icrms[PminInd]/IcMax) + 1
Ncs = round(Ncp*Cn/OptCr)    #String of capacitors in series
NcT = Ncp*Ncs                #Total number of capacitors in the matrix

print("\n------MATRIX CAPACITOR------")
print("Unit capacitor Cn:", round(Cn*10**6,4),'uF')
print("Maximum current per capacitor IcMax", IcMax,'A')
print("Capacitors in parallel Ncp:", Ncp)
print("Capacitors in series Ncs:", Ncs)
print("Total number of capacitors NcT:", NcT)

PthMOS = PcondMOS[PminInd]/2
PthDio = PdrDio[PminInd]/np.sqrt(2)
PthCr = Pcr[PminInd]/NcT

print("\n------THERMAL MANAGMENT------")
print("Thermal Power MOSFET:", round(PthMOS,4),'W')
print("Thermal Power Diode:", round(PthDio,4),'W')
print("Thermal Power Capacitor:", round(PthCr*10**3,4),'mW')

#----END OF THE CODE----
```

Next code, *"TransformerDesign.py"* as the library for the transformer calculation.

```
import numpy as np
from pylab import *
import pandas as pd

FilePath = r'C:\Users\foo\lib\\'
# - CoreDB = Database of magnetic cores
# - MaterialDB = Database of magnetic materials
CoreDB=pd.read_csv(FilePath+"CoreDatabase.csv")
MaterialDB=pd.read_csv(FilePath+"MaterialDatabase.csv")

# lmag = Magnetizing inductance
# mu0  = Magnetic permeability in vacuum
# mur  = Relative magnetic permeability
# n1   = Number of turns in the primary side
# Ae   = Core effective area.
# le   = Effective length.

def Lmag (mur, n1, ae, le):
    mu0 = 4*pi*1e-7
    lmag = mu0*mur*n1*n1*ae/le
    return lmag

# bmax = Maximum magnetic density
# vin  = Input voltage
# ton  = Switch ON time from MOSFET

def Bmax (vin, ton, n1, ae):
    if n <= 0:
        bmax = 10**6
```

```
    else:
        bmax=(vin*ton)/(n1*ae)  #Maximum magnetic flux density
    return bmax

def FindNturnsforLm (lm_ob,vin,ton,material,core):
    bsat=MaterialDB.loc[material,"Bsat @100 oC"]
    mur=MaterialDB.loc[material,"mu_r @25 oC"]
    mu0=4*pi*1e-7

    ae=CoreDB.loc[core,"Ae (m2)"]
    le=CoreDB.loc[core,"le (m)"]

    #Number of turns required for Lm.
    nclose=floor(sqrt((lm_ob*le)/(mu0*mur*ae)))
    while Lmag(mur,nclose,ae,le) > lm_ob:
        nclose = nclose - 1

    if Bmax(vin,ton, nclose, ae) >= bsat :
        lmag_final = "Saturation"
        nclosefinal = "Saturation"

    if Bmax(vin,ton, nclose, ae) < bsat :
        lmag_final = Lmag(mur,nclose,ae,le)
        nclosefinal = nclose

    return nclosefinal, lmag_final

# n_prim = Primary turns
# n_sec = Secondary turns
# Aw = Available winding area

def Wires_PP(n_prim,n_sec,wff,core,i_prim_RMS,i_dens_max):
    N = n_sec/n_prim

    Aw=CoreDB.loc[core,"Aw (m2)"]
    Aw = Aw*wff
#Minimum area required for maximum density current
    AJ_prim = i_prim_RMS/i_dens_max

    AwJ = 4*n_prim*AJ_prim

    if Aw >= AwJ:
        IncA_prim = (Aw-AwJ)/(2*(1+1/N))

        diam_prim = np.sqrt(4/np.pi*(AJ_prim+IncA_prim))
        diam_sec = diam_prim/np.sqrt(N)
    else:
        diam_prim = 0.000001 # diameter = 1 um
        diam_sec = 0.000001  # diameter = 1 um

    return diam_prim,diam_sec


def CopperLosses(n_prim,n_sec,diam_prim,diam_sec,core,i_prim_RMS):
    rho=1.68e-8  #Copper resistivity
    le=CoreDB.loc[core,"lm (m)"]
```

```
CopperLosses_prim=(rho*n_prim*le*i_prim_RMS**2)/(np.pi*diam_prim*diam_
prim/4)

CopperLosses_sec=(rho*n_sec*le*(i_prim_RMS*n_prim/n_sec)**2)/(np.pi*di
am_sec*diam_sec/4)
    CopperLosses_tot=(CopperLosses_prim+CopperLosses_sec)

    return CopperLosses_tot

def ResistanceWire(n_prim,n_sec,diam_prim,diam_sec,core):
    rho=1.68e-8
    le=CoreDB.loc[core,"lm (m)"]

    resPrim = rho*n_prim*le/(np.pi*diam_prim**2/4)
    resSec = rho*n_sec*le/(np.pi*diam_sec**2/4)

    return resPrim, resSec

def CoreLosses(n1,ton,vin,fswitch,core,material):
    ton_pp = ton

    ae=CoreDB.loc[core,"Ae (m2)"]
    vol=CoreDB.loc[core,"Ve (m3)"]

    Cm=MaterialDB.loc[material,"C"]
    alpha=MaterialDB.loc[material,"x"]
    beta=MaterialDB.loc[material,"y"]
    #Steinmetz equation
CoreLosses=float(vol)*float(Cm)*((fswitch)**float(alpha))*(((vin*ton_p
p)/(float(ae)*n1))**float(beta))

    return CoreLosses

def MinLm(ton,vin,material,core):
    bsat= MaterialDB.loc[material,"Bsat @100 oC"]
#A tolerance is included to avoid choosing the limit value
    bmax = bsat * 0.95
    mur= MaterialDB.loc[material,"mu_r @25 oC"]
    mu0= 4*pi*1e-7

    ae=CoreDB.loc[core,"Ae (m2)"]    #Magnetic effective area
    le=CoreDB.loc[core,"le (m)"]     #Effective length

    minLm =
mu0*mur*np.power(vin,2)*np.power(ton,2)/(le*ae*np.power(bmax,2))

    return minLm

def TransformerComparator(lm_ob, vin, ton, n2n1, wff, fswitch,
i_prim_RMS, i_dens_max):
    global MaterialDB #IT MUST BE GLOBAL INSIDE THE FUNCTION, if not
it wont work
    #We update the material database and choose the ones inside the
operation frequency
    MaterialDB = pd.read_csv(FilePath+"MaterialDatabase.csv")
    MaterialDB = MaterialDB[( fswitch >= MaterialDB.fmin) & (fswitch <
MaterialDB.fmax)]
    MaterialDB = MaterialDB.reset_index(drop=True)
```

```
    Rprim           = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    Rsec            = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    Cu_Losses       = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    Co_Losses       = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    Total_Losses    = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    Primary_turns   = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    Secondary_turns = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    Lm_real         = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    diam_prim       = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))
    diam_sec        = np.zeros((MaterialDB.shape[0],CoreDB.shape[0]))

    dataDB={}

    for i in range(MaterialDB.shape[0]):
        for j in range(CoreDB.shape[0]):
            if FindNturnsforLm(lm_ob,vin,ton,i,j)[1] == "Saturation" :
                Cu_Losses[i][j] = NaN
                Co_Losses[i][j] = NaN
                Total_Losses[i][j]= NaN

            else :

                (Primary_turns[i][j], Lm_real[i][j]) =
FindNturnsforLm(lm_ob,vin,ton,i,j)
                Secondary_turns[i][j] = Primary_turns[i][j]*n2n1
                diam_prim[i][j], diam_sec[i][j] =
Wires_PP(Primary_turns[i][j],Secondary_turns[i][j],wff,j,i_prim_RMS,i_
dens_max)
                Rprim[i][j], Rsec[i][j] =
ResistanceWire(Primary_turns[i][j],Secondary_turns[i][j],diam_prim[i][
j],diam_sec[i][j],j)
                Cu_Losses[i][j] =
CopperLosses(Primary_turns[i][j],Secondary_turns[i][j],diam_prim[i][j]
,diam_sec[i][j],j,i_prim_RMS)

Co_Losses[i][j]=CoreLosses(Primary_turns[i][j],ton,vin,fswitch,j,i)
                Total_Losses[i][j]=Cu_Losses[i][j]+Co_Losses[i][j]

        data={
            'Material':MaterialDB.iloc[i,0],
            'Core shape':list(CoreDB["Part"]),
            'Lm_teórica[uH]': Lm_real[i,:]*1e6,
            'N1': Primary_turns[i,:],
            'Dprim [mm]': diam_prim[i,:]*1e3,
            'N2': Secondary_turns[i,:],
            'Dsec [mm]': diam_sec[i,:]*1e3,
            'Rprim [mOhm]': Rprim[i,:]*1e3,
            'Rsec [mOhm]': Rsec[i,:]*1e3,
            'CUw [W]' : Cu_Losses[i,:],
            'COw [W]' : Co_Losses[i,:],
            'Total_losses [W]' : Total_Losses[i,:],
#Approximation of weight based on core + the copper winding
            'Weight [kg]' : CoreDB["Weight (kg)"]+CoreDB["Aw
(m2)"]*CoreDB["lm (m)"]*wff*896
                }

        dataDB[i]=pd.DataFrame(data)
```

```
    return dataDB

#----END OF THE CODE----
```

Next code, *"S3DCX Control loop.py"* which is used for the calculation of the control loop.

```
import numpy as np

#----Input parameters----

Vbus = 300          #Regulated output voltage
Isas = 4            #Short-circuit Solar array current
n = 3               #Transformer gain
ph = 1              #Number of phases in the convreter
Cbus = 400*10**-6 #Bus capacitor used
Vref = 1.225        #Reference voltage
Vhis = 1.2          #Hysteresis voltage

AVopp_max = 0.005*Vbus
Zo_max = 0.02*Vbus*n/(Isas*ph)
Cbus_min = Isas*ph/(400*np.pi*Vbus*n)
print("Maximum output ripple: ", AVopp_max, "V")
print("Maximum output impedance: ", Zo_max, "Ohm")
print("Minimum bus capacitor: ",round(Cbus_min*10**6,3), "uF")

#------------------------
#----Loop parameters----

AVopp_max = 1

k = Vref/Vbus
G = Isas/(n*Vhis)
Aer_min = (Vhis*ph)/(Vref*0.02)

AVopp_temp = Vhis/(k*Aer_min)
#Check if the obtained ripple is lower than the maximum
if(AVopp_temp >= AVopp_max):
#Gain adjusted to the maximum allowable ripple
    Aer = Vhis/(k*AVopp_max)
    AVopp = AVopp_max
else:
    Aer = Aer_min
    AVopp = AVopp_temp

fbw = (k*Aer*G)/(Cbus*2*np.pi)

ki = Aer**2*k*G/(10*Cbus)

print("Loop gain Aer: ",round(Aer,4))
print("Outpus voltage ripple: ",AVopp,"V")
print("Bandwidth fbw: ",round(fbw,2),"Hz")
print("Integrator gain ki: ", ki)

#------------------------
#----Circuit values for PI----

RA = 510
RB = RA*(1-k)/(k)
```

```
G1 = 40
G2 = Aer/(2.6*G1)

C2 = 4.7*10**-9
R2 = 1/(C2*fbw*2*np.pi/10)
R1eq = R2/G1
R1 = R1eq - (RA*RB)/(RA+RB)

R4 = 1*10**3
R3 = R4*(G2-1)
print("Ganancia G1 = ", G1)
print("Ganancia G2 = ", G2)
print("----PI Circuit values----")
print("RA = ", round(RA,0), "Ohm")
print("RB = ", round(RB*10**-3,2), "kOhm")
print("R1 = ", round(R1*10**0,2), "Ohm")
print("R2 = ", round(R2*10**-3,2), "kOhm")
print("C2 = ", round(C2*10**9,2), "nF")
print("R3 = ", round(R3*10**-3,2), "kOhm")
print("R4 = ", round(R4*10**-3,2), "kOhm")

#------------------------
#----Circuit values for PI----

Vsat_pos = 14.5  #Positive saturation voltage
Vsat_neg = 0.25  #Negative saturation voltage
difVsat = Vsat_pos - Vsat_neg

R5 = 10*10**3

R6 = R5*(difVsat/Vhis-1)
print("----Valores circuitales del comparador de histéresis----")
print("R5 = ", round(R5*10**-3,2), "kOhm")
print("R6 = ", round(R6*10**-3,2), "kOhm")

#----END OF THE CODE----
```

Annex IV

List of semiconductors used for FoM analysis

In this annex is presented a complete list of the semiconductors used for the FoM analysis based on their electrical parameters that was presented in Section 4.4.1.

Table 20. Complete list of FETs analysed regarding their FoM.

Component	Manufacturer	Semiconductor	V_{DS} $[V]$	$R_{DS_{on}}$ $[m\Omega]$	C_{oss} $[pF]$
BUY25CS12	Infineon	Si	250	130	80
BUY25CS54A	Infineon	Si	250	30	500
BUY65CS28A	Infineon	Si	650	150	120
GS-065-018-2-L	GaN Systems	GaN	650	78	70
GS-065-030-2-L	GaN Systems	GaN	650	50	100
GS66504B	GaN Systems	GaN	650	100	40
GS66506T	GaN Systems	GaN	650	67	80
GS66508B	GaN Systems	GaN	650	50	80
GS-065-060-5-B-A	GaN Systems	GaN	650	25	250
GS66516B	GaN Systems	GaN	650	25	250
SGT120R65AL	STM	GaN	650	72	70
SGT65R65AL	STM	GaN	650	49	150
IGT60R042D1	Infineon	GaN	600	33	100
IGLR60R340D1	Infineon	GaN	600	270	18
IGLD60R070D1	Infineon	GaN	600	55	75
PGA26E07BA	Panasonic	GaN	600	56	142
PGA26E19BA	Panasonic	GaN	600	140	56
EPC7007	EPC	GaN RadHard	200	17	200
EPC7020	EPC	GaN RadHard	200	8	400
SCT055W65G3-4AG	STM	SiC	650	58	80

SCT040H65G3	STM	SiC	650	40	150
SCTW35N65G2VAG	STM	SiC	650	55	175
SCT018H65G3AG	STM	SiC	650	20	250
SCT027W65G1	STM	SiC	650	29	200
SCTW100N65G2AG	STM	SiC	650	26	350
SCTH90N65G2V	STM	SiC	650	24	375
SCTWA90N65G2V	STM	SiC	650	18	375
SCTWA70N120G2V	STM	SiC	1200	30	310
SCT020W120G3	STM	SiC	1200	18,5	290
SCT20N120	STM	SiC	1200	169	100
IMBG65R163M1H	Infineon	SiC	650	163	50
IMW65R107M1H	Infineon	SiC	650	107	65
IMW65R083M1H	Infineon	SiC	650	83	80
IMW65R072M1H	Infineon	SiC	650	72	100
IMW65R057M1H	Infineon	SiC	650	57	120
IMW65R048M1H	Infineon	SiC	650	48	150
IMW65R039M1H	Infineon	SiC	650	39	190
IMW65R030M1H	Infineon	SiC	650	30	210
IMW65R027M1H	Infineon	SiC	650	27	280
IMBG65R022M1H	Infineon	SiC	650	22	300
IMT65R022M1H	Infineon	SiC	650	22	300
IMZA120R030M1H	Infineon	SiC	1200	30	200

IMW120R020M1H	Infineon	SiC	1200	19	310
IMW120R014M1H	Infineon	SiC	1200	14	420
AIMBG120R010M1	Infineon	SiC	1200	8,7	500
IMW120R007M1H	Infineon	SiC	1200	7	850
C2M0080120D	Wolfspeed	SiC	1200	80	150
TP65H015G5WS	Transphorm	GaN Cascode	650	18	400
TP65H035G4WS	Transphorm	GaN Cascode	650	35	210
TP65H050G4WS	Transphorm	GaN Cascode	650	50	180
TP65H070G4PS	Transphorm	GaN Cascode	650	72	100
TP65H150G4PS	Transphorm	GaN Cascode	650	150	42
GAN041-650WSB	Nexperia	GaN Cascode	650	35	210
GAN039-650NBB	Nexperia	GaN Cascode	650	33	200
GAN111-650WSB	Nexperia	GaN Cascode	650	97	60
UG4SC075011K4S	Qorvo	SiC Cascode	750	10	220
UG3SC120009K4S	Qorvo	SiC Cascode	1200	7,6	500
UG4SC075009K4S	Qorvo	SiC Cascode	750	8,4	300

Table 21. Complete list of diodes analysed regarding their FoM.

Component	Manufacturer	Semiconductor	V_{RRM} $[V]$	V_f $[V]$	Q_C $[nC]$
STTH60400HR	STM	Si RadHard	400	0,78	1400
STPSC5H12	STM	SiC	1200	1,56	30
STPSC10H12	STM	SiC	1200	1,25	47,5
STPSC15H12	STM	SiC	1200	1,12	80
STPSC20H12	STM	SiC	1200	1,1	110
C4D05120E	Wolfspeed	SiC	1200	1,65	22,5
C4D08120E	Wolfspeed	SiC	1200	1,5	34
E4D10120A	Wolfspeed	SiC	1200	1,25	44
C4D15120H	Wolfspeed	SiC	1200	1,25	65
C4D20120H	Wolfspeed	SiC	1200	1,2	82
C4D30120H	Wolfspeed	SiC	1200	1,25	65
C4D40120H	Wolfspeed	SiC	1200	1	160
C6D05170H	Wolfspeed	SiC	1200	1,5	40
C6D10170H	Wolfspeed	SiC	1700	1,25	68
C6D25170H	Wolfspeed	SiC	1700	1,1	180
IDM08G120C5	Infineon	SiC	1200	1,5	17
IDWD15G120C5	Infineon	SiC	1200	1,2	50
IDH16G120C5	Infineon	SiC	1200	1,25	33
IDH20G120C5	Infineon	SiC	1200	1,1	50

Annex V

Software digital control for single power cell

In this annex is presented the software, which was implemented in *Verilog* using *IceStudio*, used for the switching control of the power cell during the vacuum tests as presented in Chapter 4.

The code for the counter module is presented as follows.

```
localparam N = 14;
localparam S0 = 0, S1 = 1;

reg[0:0] state_reg, state_next;
reg[0:0] bf_signal, rst;

reg[N-1:0] counter = 0;

always @(posedge clk_in) begin
    if(rst) begin
        counter <= 0;
        state_reg <= state_next;
    end else begin
        counter <= counter + 1;
    end
end

always @* begin
    state_next = state_reg;
    case(state_reg)
        S0: begin
            if(counter >= (tgapC - 1)) begin
                state_next <= S1;
                rst <= 1;
                bf_signal <= 1;
            end else begin
                state_next <= S0;
                bf_signal <= 0;
                rst <= 0;
            end
        end
        S1: begin
            if(counter >= (tonC - 1)) begin
                state_next <= S0;
                rst <= 1;
                bf_signal <= 0;
            end else begin
                state_next <= S1;
                bf_signal <= 1;
                rst <= 0;
            end
        end
        default: state_next <= S0;
    endcase
end

assign driving_out = bf_signal;

//----END OF THE CODE----
```

The code for the selector module is presented.

```
localparam state0 = 2'b00,
           state1 = 2'b01,
           state2 = 2'b10;

reg[0:0] sel = 0;
reg[1:0] CurrentState = 00;
reg[1:0] NextState = 00;

always @(negedge clk_in) begin
    CurrentState = NextState;
    case (CurrentState)
        state0: begin
            if (s0 == 1)
                NextState = state1;
        end
        state1: begin
            if (s0 == 0) begin
                NextState = state2;
            end
        end
        state2: begin
            sel = ~ sel;
            NextState = state0;
        end
    endcase
end

assign o1 = sel ? 0 : s0;
assign o2 = sel ? s0 : 0;
assign debug = NextState[1];

//----END OF THE CODE----
```